Migrating from AT89S8252/S53 to AT89S8253

New Features

- 64-byte User Signature Array
- Enhanced UART with Frame Detection and Automatic Address Recognition
- Enhanced SPI (Double Write/Read Buffered) Serial Interface
- Page Mode in both Parallel/Serial Programming Modes (Code/Data Memories)
- Four-level Enhanced Interrupt Controller
- Programmable and Fuseable x2 Clock Option
- Internal Power-on Reset
- 42-pin PDIP Package Option for Reduced EMI Emission
- EEPROM Page Write Access during CPU Execution

Introduction

The purpose of this application note is to help users convert existing designs from AT89S8252/S53 to AT89S8253. The given information will also help migration from AT89LS8252/LS53 to AT89S8253. This application note describes AT89S8253 memory sizes, features, and SFR mapping. More detailed information can be found in the AT89S8253 datasheet.

Memory Sizes

The following table shows a comparison of the individual memories.

Memory	AT89S8252	AT89S53	AT89S8253
Flash	8K Bytes	12K Bytes	12K Bytes
RAM	256 Bytes	256 Bytes	256 Bytes
EEPROM	2K Bytes	N/A	2K Bytes

64-byte User Signature Array

Sixty-four bytes are accessible to the user to program their own desired data. Bytes can be either programmed by parallel or serial mode.

Flash Microcontrollers

Application Note

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Enhanced UART with Frame Error Detection and Automatic Address Recognition

When used for frame error detection, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON Register. Automatic Address Recognition allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparison.

Enhanced SPI (Double Write/Read Buffered) Serial Interface

The enhanced SPI mode allows the write buffer to hold the next byte to be transmitted. As long as the CPU can keep the write buffer full, multiple bytes may be transferred with minimal latency between bytes.

Page Mode in both Parallel/Serial Programming Modes (Code/Data Memories)

Program and data memories can be programmed in page mode (1 code page = 64 bytes; data page = 32 bytes).

Page mode is available in both the parallel and serial programming modes.

Four-level Enhanced Interrupt Controller

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority (IP) register and in the Interrupt Priority High (IPH) register.

The Interrupt Priority High register shows the bit values and priority levels associated with each combination.

Programmable and Fuseable x2 Clock Option

The x2 clock option allows the microcontroller to execute one machine cycle in 6 clock periods instead of 12 clock periods. This can be set either through hardware or software.

Internal Power-On Reset

A 1 ms internal reset signal will be generated after power-on, eliminating the need for any external Power-on reset circuitry.

42-pin PDIP Package Option for Reduced EMI Emission

The 42-pin package has extra pins PWRVDD and PWRGND to reduce EMI Emission. PWRVDD must be connected to the application board supply voltage. PWRGND must be connected to the application board GND.

EEPROM Page Write during CPU Execution

During CPU execution, EEPROM can be written one page (32 bytes) at a time. This way, 32 bytes will only require 4 ms of programming time instead of 128 ms required in single byte programming.

Operational V_{CC} Voltage Range

While the AT89S8252/S53 are offered in low-voltage versions as AT89LS8252/LS53, respectively, the AT89S8253 nomenclature encompasses both the regular (4.0V to 5.5V) and low-voltage (2.7V to 4.0V) operational V_{CC} voltage ranges. The ordering is designated by the appropriate operational frequency range. Please consult the Ordering Information table in the AT89S8253 device datasheet.

SFRs Mapping

The highlighted SFR locations are new registers for the AT89S8253 device.

0F8H									0FFH
0F0H	B								0F7H
0E8H									0EFH
0E0H	ACC								0E7H
0D8H									0DFH
0D0H	PSW					SPCR			0D7H
0C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			0CFH
0C0H									0C7H
0B8H	IP	SADEN							0BFH
0B0H	P3							IPH	0B7H
0A8H	IE	SADDR	SPSR						0AFH
0A0H	P2						WDTRST	WDTCON	0A7H
98H	SCON	SBUF							9FH
90H	P1						EECON		97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	CLKREG	8FH
80H	P0	SP	DP0L	DP0H	DP1L	DP1H	SPDR	PCON	87H

Note: **1.** In the AT89S8253, the DP0L/H register pair always accesses DPTR0 and the DP1L/H pair always accesses DPTR1 regardless of the state of the DPS bit in SFR EECON. This is different than in the AT89S8252/AT89S53 devices, where the DPL/H switch between DPTR0 and DPTR1 is based on the state of the DPS bit. For further information on the dual data pointer usage, refer to the AT89S8253 datasheet and to the application note titled “AT89S8252 Primer” located in Atmel’s web site.

Fuse Table

Fuse	AT89S8252	AT89S53	AT89S8253
SerialProg	Yes	Yes	Yes
x2 Clock	No	No	Yes
UserRowProg	No	No	Yes

Programming Time (Byte Mode)

Part Number	Flash (Reset = High)	EEPROM (Reset = High)	EEPROM Reset = Low (CPU Execution)
AT89S8252	12 sec	2.7 sec	5.12 sec
AT89S53	16 sec	N/A	N/A
AT89S8253	N/A	N/A	N/A

Programming Time (Page Mode)

Part Number	Flash (Reset = High)	EEPROM (Reset = High)	EEPROM Reset = Low (CPU Execution)
AT89S8252	N/A	N/A	N/A
AT89S53	N/A	N/A	N/A
AT89S8253	0.96 sec	0.32 sec	0.256 sec

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