#### **Features**

- Read Access Time 90 ns
- Word-wide or Byte-wide Configurable
- 8-Megabit Flash and Mask ROM Compatable
- Low Power CMOS Operation
  - 100 µA Maximum Standby
  - 50 mA Maximum Active at 5 MHz
- Wide Selection of JEDEC Standard Packages
  - 42-Lead 600 mil PDIP
  - 44-Lead PLCC
  - 44-Lead SOIC (SOP)
  - 48-Lead TSOP (12 mm x 20 mm)
- 5V ± 10% Power Supply
- High Reliability CMOS Technology
  - 2,000 ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm 50 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

### Description

The AT27C800 is a low-power, high performance 8,388,608-bit UV erasable programmable read only memory (EPROM) organized as either 512K by 16 or 1024K by 8 (continued)

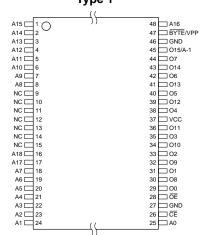
# **Pin Configurations**

Pin Name	Function			
A0 - A18	Addresses			
O0 - O15	Outputs			
O15/A-1	Output/Address			
BYTE/VPP	Byte Mode/ Program Supply			
CE	Chip Enable			
OE	Output Enable			
NC	No Connect			

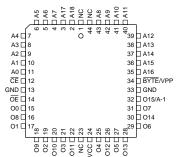
PD	IP Top	۱ ر	/iew	SC	DIC (S	OP)
	$\overline{}$		1			_
A18 🗆	1	42	□ NC	NC 🗆	1	44 🗀 NC
A17 □	2	41	□ A8	A18 🗆	2	43 = NC
A7 □	3	40	□ A9	A17 🗆	3	42 A8
A6 □	4	39	□ A10	A7 🗆	4	41 A9
A5 □	5	38	□ A11	A6 🗆	5	40 A10
A4 🗆	6	37	□ A12	A5 🗀	6	39 A11
A3 🗆	7	36	□ A13	A4 🗀	7	38 A12
A2 🗆	8	35	□ A14	A3 🗀	8	37 A13
A1 🗆	9	34	□ A15	A2 🗀	9	36 A14
A0 🗆			□ A16	A1 🗀	10	35 A15
CE [	11	32	□ BYTE/VPP	A0 🗀	11	34 A16
GND 🗆		31	□GND	Œ □	12	33 BYTE/VPP
OE [	1 -		O15/A-1	GND □	13	32 GND
00 □	1		D 07	ŌE 🗆	14	31 O15/A-1
08 □	1 -		014	00 🗆	15	30 🗖 07
O1 [	1 -		□ 06	O8 🗀	16	29 O14
O9 🗆	1	26	□ O13	01 🗀	17	28 O6
O2 [		25	□ 05	O9	18	27 🔲 013
O10 🗆			D 012	O2	19	26 O5
O3 [	ı		□ 04	O10 🗀	20	25 🗆 012
011 □	21	22	□ vcc	O3 🗀	21	24 🗆 04
				011 □	22	23 VCC



Type 1



**PLCC Top View** 



Note: PLCC Package Pin 23 is DON'T CONNECT.





8-Megabit (512K x 16 or 1024K x 8) OTP EPROM

AT27C800

Rev. 0801B-10/98



bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 90 ns, eliminating the need for speed-reducing WAIT states. The x16 organization makes this part ideal for high-performance 16- and 32-bit microprocessor systems.

The AT27C800 can be organized as either word-wide or byte-wide. The organization is selected via the  $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$  pin. When  $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$  is asserted high (V<sub>IH</sub>), the word-wide organization is selected and the O15/A-1 pin is used for O15 data output. When  $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$  is asserted low (V<sub>IL</sub>),the byte wide organization is selected and the O15/A-1 pin is used for the address pin A-1. When the AT27C800 is logically regarded as x16 (word-wide), but read in the byte-wide mode, then with A-1=V<sub>IL</sub> the lower eight bits of the 16 bit word are selected with A-1 =V<sub>IH</sub> the upper 8 bits of the 16-bit word are selected.

In read mode, the AT27C800 typically consumes 15 mA. Standby mode supply current is typically less than 10  $\mu\text{A}.$ 

The AT27C800 is available in industry standard JEDEC-approved one-time programmable (OTP) PLCC, PDIP, SOIC (SOP), and TSOP as well as UV erasable windowed Cerdip packages. The device features two-line control(CE,OE) to eliminate bus contention in high-speed systems.

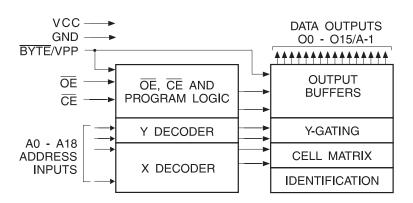
With high density 512K word or 1024K-bit storage capability, the AT27C800 allows firmware to be to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C800 has additional features that ensure high quality and efficient production use. The Rapid<sup>TM</sup> Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50μs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming equipment and voltages.

### **System Considerations**

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu F$  high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu F$  bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

# **Block Diagram**



## **Absolute Maximum Ratings\***

Temperature Under Bias5	55°C to +125°C
Storage Temperature	65°C to +150°C
Voltage on Any Pin with with Respect to Ground2	2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground2.	0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground2.	0V to +14.0V <sup>(1)</sup>

\*NOTICE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device

reliability.

Note: Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V DC which may overshoot to + 7.0V for pulses of less than 20 ns.

### **Operating Modes**

						Outputs	
Mode\Pin	CE	ŌĒ	Ai	BYTE/V <sub>PP</sub>	O <sub>0</sub> -O <sub>7</sub>	O <sub>8</sub> -O <sub>14</sub>	O <sub>15</sub> /A-1
Read Word-wide	V <sub>IL</sub>	V <sub>IL</sub>	X <sup>(1)</sup>	V <sub>IH</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>
Read Byte-wide Upper	V <sub>IL</sub>	V <sub>IL</sub>	X <sup>(1)</sup>	$V_{IL}$	D <sub>OUT</sub>	High Z	$V_{IH}$
Read Byte-wide Lower	V <sub>IL</sub>	V <sub>IL</sub>	X <sup>(1)</sup>	V <sub>IL</sub>	D <sub>OUT</sub>	High Z	V <sub>IL</sub>
Output Disable	X <sup>(1)</sup>	V <sub>IH</sub>	X <sup>(1)</sup>	Х		High Z	
Standby	V <sub>IH</sub>	X <sup>(1)</sup>	X <sup>(1)</sup>	X <sup>(5)</sup>		High Z	
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>		D <sub>IN</sub>	
PGM Verify	Х	V <sub>IL</sub>	Ai	V <sub>PP</sub>		D <sub>OUT</sub>	
PGM Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	X <sup>(1)</sup>	V <sub>PP</sub>		High Z	
Product Identification <sup>(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	$A9 = V_H^{(3)}$ $A0 = V_{IH} \text{ or } V_{IL}$ $A1 - A18 = V_{IL}$	V <sub>IH</sub>	lde	ntification (	Code

Notes:

- 1. X can be V<sub>IL</sub> or V<sub>IH.</sub>
- 2. Refer to the programming characteristics tables in this data sheet.
- 3.  $V_H = 12.0 \pm 0.5 V$ .
- 4. Two identifier words may be selected. All Ai inputs are held low (V<sub>IL</sub>) except A9, which is set to V<sub>H</sub>, and A0, which is toggled low  $(V_{IL})$  to select the Manufacturer's Identification word and high  $(V_{IH})$  to select the Device Code word.
- 5. Standby  $V_{CC}$  current ( $I_{SB}$ ) is specified with  $V_{PP} = V_{CC}$ .  $V_{CC} > V_{PP}$  will cause a slight increase in  $I_{SB}$ .





# **DC and AC Operating Conditions for Read Operation**

			AT27C800						
		-90	-10	-12	-15				
Operating	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C				
Temperature (Case)	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C				
V <sub>CC</sub> Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%				

# **DC and Operating Characteristics for Read Operation**

Symbol	Parameter	Condition	Min	Max	Units
ILI	Input Load Current	$V_{IN} = 0V \text{ to } V_{CC}$		±1.0	μΑ
I <sub>LO</sub>	Output Leakage Current	$V_{OUT} = 0V \text{ to } V_{CC}$		±5.0	μΑ
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	$V_{PP} = V_{CC}$		±10	μΑ
	V (1) Standby Current	$I_{SB1}$ (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μΑ
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	$I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V		1.0	mA
	V <sub>CC</sub> Active Current	$f = 5MHz$ , $I_{OUT} = 0$ mA, $\overline{CE} = V_{IL}$		50	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 mA	2.4		V

Notes: 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .

# **AC Characteristics for Read Operation**

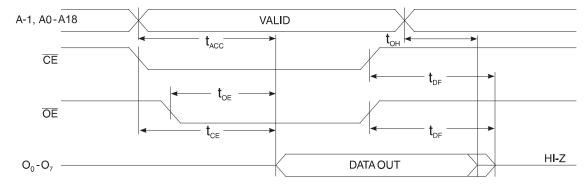
						AT27	C800				
			-(	90	-1	10	-1	12	-1	15	
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t <sub>ACC</sub> <sup>(3)</sup>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90		100		120		150	ns
t <sub>CE</sub> <sup>(2)</sup>	CE to Output Delay	OE = V <sub>IL</sub>		90		100		120		150	ns
t <sub>OE</sub> <sup>(2,3)</sup>	OE to Output Delay	CE = V <sub>IL</sub>		40		40		40		50	ns
t <sub>DF</sub> <sup>(4,5)</sup>	OE or CE High to Output Floa occured first	t, whichever		30		30		35		40	ns
t <sub>OH</sub> <sup>(4)</sup>	Output Hold from Address CE whichever occured first	or <del>OE</del> ,	5.0		5.0		5.0		5.0		ns
t <sub>ST</sub>	BYTE High to Output Valid			90		100		120		150	ns
t <sub>STD</sub>	BYTE Low to Output Transition	n		40		40		50		60	ns

Note: 2,3,4,5. See the AC Waveforms for Read Operation diagram.

Preliminary Information

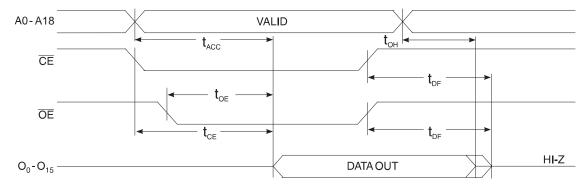
<sup>2.</sup>  $V_{PP}$  may be connected directly to  $V_{CC}$  except during programming. The supply current would then be the sum of  $I_{CC}$  and  $I_{PP}$ .

# Byte-Wide Read Mode AC Waveforms<sup>(1)</sup>



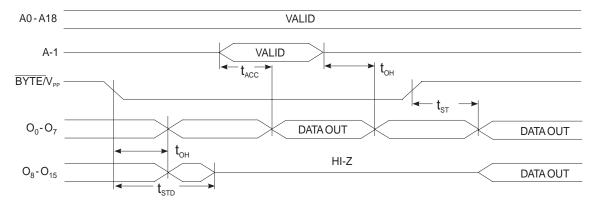
Note: 1.  $\overline{\text{BYTE}}/\text{V}_{PP} = \text{V}_{IL}$ 

# Byte-Wide Read Mode AC Waveforms<sup>(1)</sup>



Note: 1.  $\overline{BYTE}/V_{PP} = V_{IH}$ 

# **BYTE** Transition AC Waveforms



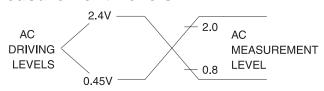
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.

- 2.  $\overline{\text{OE}}$  may be delayed up to  $t_{\text{CE}}$   $t_{\text{OE}}$  after the falling edge of  $\overline{\text{CE}}$  without impact on  $t_{\text{CE}}$ .
- OE may be delayed up to t<sub>ACC</sub> t<sub>OE</sub> after the address is valid without impact on t<sub>ACC</sub>.
- 4. This parameter is only sampled and is not 100% tested.
- 5. Output float is defined as the point when data is no longer driven.



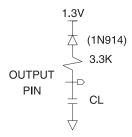


# **Input Test Waveforms and Measurement Levels**



 $t_R$ ,  $t_F$  < 20 ns (10% to 90%)

## **Output Test Load**



Note: CL = 100 pF including jig capacitance.

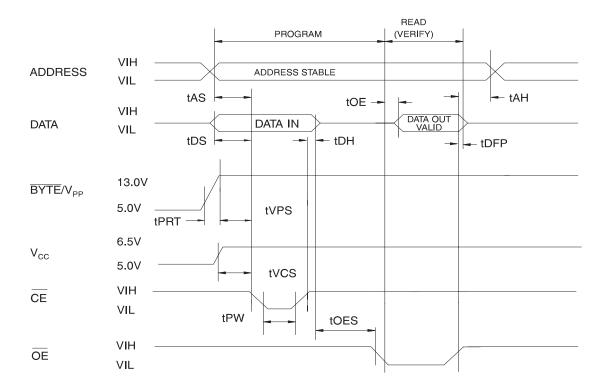
# **Pin Capacitance**

 $f = 1 \text{ MHz}, T = 25^{\circ}C^{(1)}$ 

Symbol	Тур	Max	Units	Conditions
C <sub>IN</sub>	4	10	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	8	12	pF	V <sub>OUT</sub> = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

# **Programming Waveforms**<sup>(1)</sup>



Notes: 1. The Input Timing reference is 0.8V for  $V_{\rm IL}$  and 2.0V for  $V_{\rm IH}$ .

- 2.  $t_{\text{OE}}$  and  $t_{\text{DFP}}$  are characteristics of the device but must be accommodated by the programmer.
- 3. When programming the AT27C800, a 0.1  $\mu F$  capacitor is required across  $V_{pp}$  and ground to suppress voltage transients.

# **DC Programming Characteristics**

 $T_A = 25 \pm 5^{\circ}C$ ,  $V_{CC} = 6.5 \pm 0.25V$ ,  $V_{PP} = 13.0 \pm 0.25V$ 

			Lin	nits	
Symbol	Parameter	Test Conditions	Min	Max	Units
ILI	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	μΑ
V <sub>IL</sub>	Input Low Level		-0.6	0.8	٧
V <sub>IH</sub>	Input High Level		2.0	V <sub>CC</sub> + 0.5	٧
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	٧
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		٧
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Program and Verify)			50	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	CE = V <sub>IL</sub>		30	mA
V <sub>ID</sub>	A9 Product Identification Voltage		11.5	12.5	V



# **AC Programming Characteristics**

 $T_A = 25 \pm 5^{\circ}C, \ V_{CC} = 6.5 \pm 0.25V, \ V_{PP} = 13.0 \pm 0.25V$ 

•			Lir		
Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Units
t <sub>AS</sub>	Address Setup Time	Input Rise and Fall Times:	2		μs
t <sub>OES</sub>	OE Setup Time	(10% to 90%) 20 ns	2		μs
t <sub>DS</sub>	Data Setup Time		2		μs
t <sub>AH</sub>	Address Hold Time	Input Pulse Levels:  45V to 2.4V	0		μs
t <sub>DH</sub>	Data Hold Time	70 V to 2.4 V	2		μs
t <sub>DFP</sub>	OE High to Output Float Delay <sup>(2)</sup>	Input Pulse Levels:	0	130	ns
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	0.8V to 2.0V	2		μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	Input Timing Reference Level:	2		μs
t <sub>PW</sub>	CE Program Pulse Width <sup>(3)</sup>	0.8V to 2.0V	47.5	52.5	μs
t <sub>OE</sub>	Data Valid from OE	Outsid Timin a Defense		150	ns
t <sub>PRT</sub>	BYTE N <sub>PP</sub> Pulse Rise Time During Programming	Output Timing Reference Level:  0.8V to 2.0V	50		ns

Notes: 1.  $V_{cc}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

# **Atmel's 27C800 Integrated Product Identification Code**

Pins										
	A0	O15	014	O13	O12	011	O10	О9	08	
Codes		07	06	O5	04	О3	02	01	00	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E1E
Device Type	1	1	1	1	1	1	0	0	0	F8F8

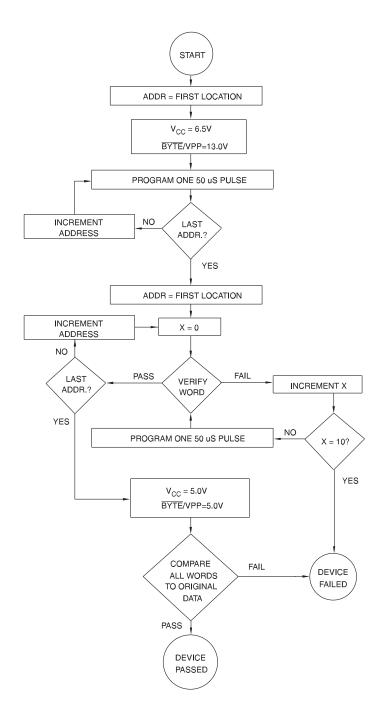
<sup>2.</sup> This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

<sup>3.</sup> Program Pulse width tolerance is 50  $\mu$ s  $\pm$  5%.

### **Rapid Programming Algorithm**

A 50  $\mu$ s  $\overline{\text{CE}}$  pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5V and  $\overline{\text{BYTE}}/V_{PP}$  is raised to 13.0V. Each address is first programmed with one 50  $\mu$ s  $\overline{\text{CE}}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50  $\mu$ s pulses are applied with a verification after each

pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked.  $V_{\text{PP}}$  is then lowered to 5.0V and  $V_{\text{CC}}$  to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.







# **Ordering Information**

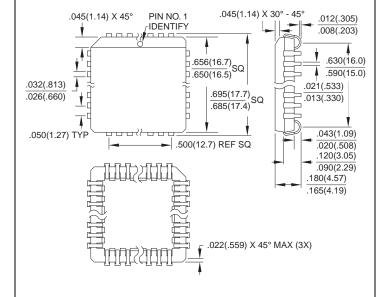
t <sub>ACC</sub>	I <sub>cc</sub>	(mA)			
(ns)	Active	Standby	Ordering Code	Package	Operation Range
90	50	0.1	AT27C800-90JC	44J	Commercial
			AT27C800-90PC	42P6	(0°C to 70°C)
			AT27C800-90RC	44R	
			AT27C800-90TC	48T	
	50	0.1	AT27C800-90JI	44J	Industrial
			AT27C800-90PI	42P6	(-40°C to 85°C)
			AT27C800-90RI	44R	
			AT27C800-90TI	48T	
100	50	0.1	AT27C800-10JC	44J	Commercial
			AT27C800-10PC	42P6	(0°C to 70°C)
			AT27C800-10RC	44R	
			AT27C800-10TC	48T	
	50	0.1	AT27C800-10JI	44J	Industrial
			AT27C800-10PI	42P6	(-40°C to 85°C)
			AT27C800-10RI	44R	
			AT27C800-10TI	48T	
120	50	0.1	AT27C800-12JC	44J	Commercial
			AT27C800-12PC	42P6	(0°C to 70°C)
			AT27C800-12RC	44R	
			AT27C800-12TC	48T	
	50	0.1	AT27C800-12JI	44J	Industrial
			AT27C800-12PI	42P6	(-40°C to 85°C)
			AT27C800-12RI	44R	
			AT27C800-12TI	48T	
150	50	0.1	AT27C800-15JC	44J	Commercial
			AT27C800-15PC	42P6	(0°C to 70°C)
			AT27C800-15RC	44R	
			AT27C800-15TC	48T	
	50	0.1	AT27C800-15JI	44J	Industrial
			AT27C800-15PI	42P6	(-40°C to 85°C)
			AT27C800-15RI	44R	
			AT27C800-15TI	48T	

Preliminary Information

Package Type	
44J	44-Lead, Plastic J Leaded Chip Carrier (PLCC)
42P6	42-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44R	44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)
48T	48-Lead, Plastic Thin Small Outline Package (TSOP) 12 x 20 mm

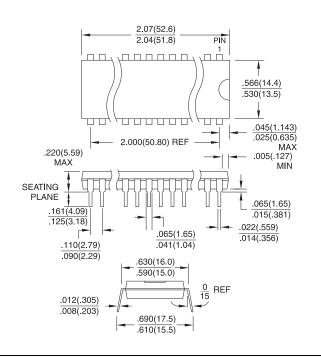
## **Packaging Information**

**44J**, 44-Lead, Plastic J Leaded Chip Carrier (PLCC) Dimensions in Inches and (Millimeters)



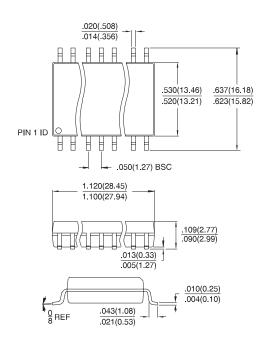
**42P6**, 42-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Dimensions in Inches and (Millimeters)



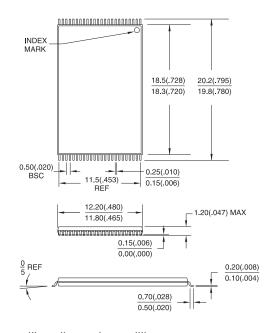
**44R**, 44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)

Dimensions in Inches and (Millimeters)



**48T**, 48-Lead, Plastic Thin Small Outline Package (TSOP)

Dimensions in Millimeters and (Inches)\*
JEDEC OUTLINE MO-142 DD



\*Controlling dimension: millimeters





### **Atmel Headquarters**

Corporate Headquarters

2325 Orchard Parkway San Jose, CA 95131 TEL (408) 441-0311 FAX (408) 487-2600

#### **Europe**

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

#### Asia

Atmel Asia, Ltd. Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon, Hong Kong TEL (852) 27219778 FAX (852) 27221369

#### Japan

Atmel Japan K.K. Tonetsu Shinkawa Bldg., 9F 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan TEL (81) 3-3523-3551 FAX (81) 3-3523-7581

### **Atmel Operations**

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 TEL (719) 576-3300 FAX (719) 540-1759

#### Atmel Rousset

Zone Industrielle 13106 Rousset Cedex, France TEL (33) 4 42 53 60 00 FAX (33) 4 42 53 60 01

> Fax-on-Demand North America: 1-(800) 292-8635 International: 1-(408) 441-0732

*e-mail* literature@atmel.com

Web Site http://www.atmel.com

*BBS* 1-(408) 436-4309

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