DS1337
Serial Real-Time Clock

www.maxim-ic.com

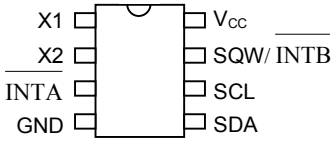
FEATURES

- Real-time clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- Two-wire serial interface
- Two time-of-day alarms
- Oscillator stop flag
- Programmable square-wave output
  – Defaults to 32kHz on power-up
- Available in 8-pin DIP, SO, or µSOP

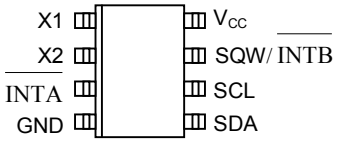
ORDERING INFORMATION

DS1337	8-Pin DIP (300mil)
DS1337S	8-Pin SO (150mil)
DS1337U	8-Pin µSOP

PIN ASSIGNMENT



8-Pin DIP (300mil)



8-Pin SO (150mil)
8-Pin µSOP

Package dimension information can be found at:
www.maxim-ic.com/TechSupport/DallasPackInfo.htm

PIN DESCRIPTION

V_{CC}	- Power Supply
X1, X2	- 32.768kHz Crystal Connection
GND	- Ground
SDA	- Serial Data
SCL	- Serial Clock
$\overline{INTA}$	- Interrupt Output
SQW/$\overline{INTB}$	- Square-Wave/Interrupt Output

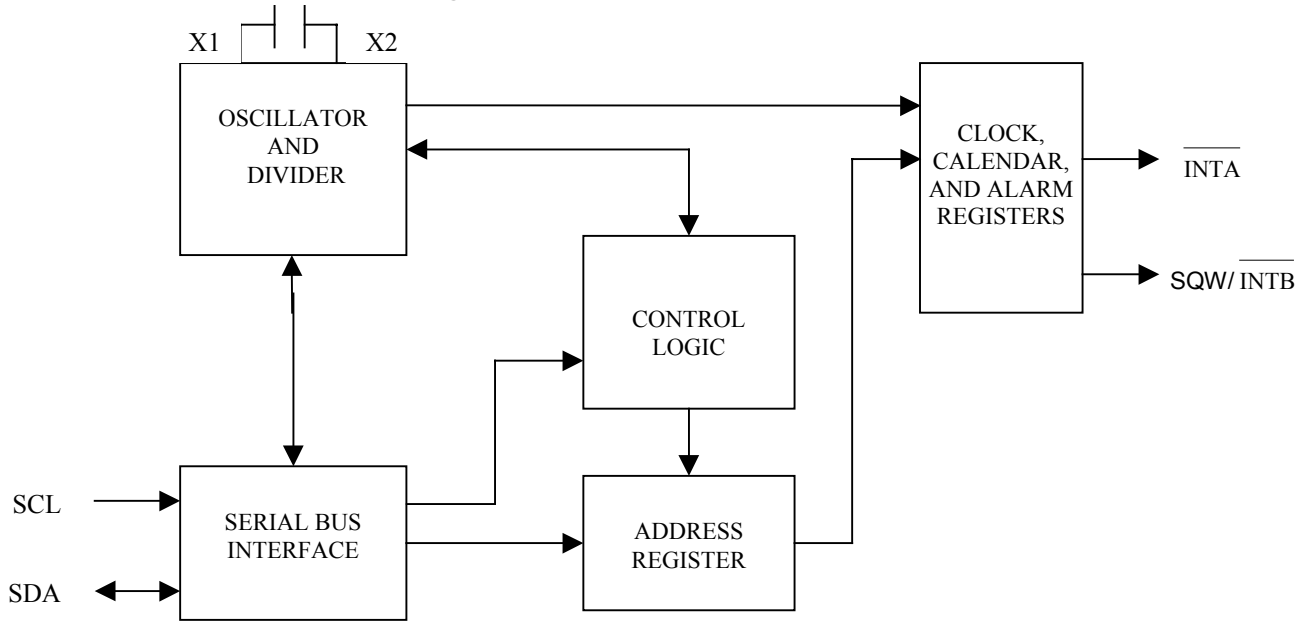
DESCRIPTION

The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially via a 2-wire, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

OPERATION

The block diagram in Figure 1 shows the main elements of the DS1337. As shown, communications to and from the DS1337 occur serially over a 2-wire, bidirectional bus. The DS1337 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed.

DS1337 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC}, GND – DC power is provided to the device on these pins.

SCL (Serial Clock Input) – SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) – SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pullup resistor.

$\overline{\text{INTA}}$ (Interrupt Output) – When enabled, $\overline{\text{INTA}}$ will be asserted low when the time/day/date matches the values set in the alarm registers. The $\overline{\text{INTA}}$ pin is an open-drain output and requires an external pullup resistor.

SQW/$\overline{\text{INTB}}$ (Square-Wave/Interrupt Output) – Programmable square-wave or interrupt output signal. The SQW/$\overline{\text{INTB}}$ pin is an open-drain output and requires an external pullup resistor.

X1, X2 – These signals are connections for a standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF.

For more information about crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real-Time Clocks." The DS1337 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

ADDRESS MAP

The address map for the registers of the DS1337 is shown in Figure 2. During a multibyte access, when the address pointer reaches the end of the register space (0Fh) it wraps around to location 00h. On a 2-wire START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

DS1337 TIMEKEEPER REGISTERS Figure 2

ADDRESS	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	FUNCTION	RANGE
00H	0	10 SECONDS			SECONDS				Seconds	00-59
01H	0	10 MINUTES			MINUTES				Minutes	00-59
02H	0	12/24	AM/PM 10HR	10HR	HOUR				Hours	1-12 +AM/PM 00-23
03H	0	0	0	0	0	DAY			Day	1-7
04H	0	0	10 DATE		DATE				Date	00-31
05H	CENTURY	0	0	10 MO	MONTH				Month/ Century	01-12 + Century
06H	10 YEAR				YEAR				Year	00-99
07H	A1M1	10 SECONDS			SECONDS				Alarm 1 Seconds	00-59
08H	A1M2	10 MINUTES			MINUTES				Alarm 1 Minutes	00-59
09H	A1M3	12/24	AM/PM 10HR	10HR	HOUR				Alarm 1 Hours	1-12 + AM/PM 00-23
0AH	A1M4	DY/DT	10 DATE		DAY DATE				Alarm 1 Day Alarm 1 Date	1-7 1-31
0BH	A2M2	10 MINUTES			MINUTES				Alarm 2 Minutes	00-59
0CH	A2M3	12/24	AM/PM 10HR	10HR	HOUR				Alarm 2 Hours	1-12 + AM/PM 00-23
0DH	A2M4	DY/DT	10 DATE		DAY DATE				Alarm 2 Day Alarm 2 Date	1-7 1-31
0EH	$\overline{\text{EOSC}}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	

Note: Unless otherwise specified, the state of the registers are not defined when power is first applied or V_{CC} falls below the V_{OSC}.

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Figure 2. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The DS1337 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

ALARMS

The DS1337 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Figure 3). When all of the mask bits for each alarm are logic 0, an alarm will only occur when the values in the timekeeping registers 00h to 06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Figure 3 shows the possible settings. Configurations not listed in the table will result in illogical operation.

The DY/DT bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY/DT is written to a logic 0, the alarm will be the result of a match with date of the month. If DY/DT is written to a logic 1, the alarm will be the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{\text{INTA}}$ or SQW/ $\overline{\text{INTB}}$) signals.

ALARM MASK BITS Figure 3

DY/DT	Alarm1 Register Mask Bits (Bit 7)				Alarm Rate
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/DT	ALARM 2 Register Mask Bits (Bit 7)			Alarm Rate
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 sec. of every min.)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL PURPOSE REGISTERS

The DS1337 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

CONTROL REGISTER (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{EOSC}}$	0	0	RS2	RS1	INTCN	A2IE	A1IE

$\overline{\text{EOSC}}$ (Enable Oscillator) – This bit when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

RS2 and RS1 (Rate Select) – These bits control the frequency of the square-wave output when the square wave has been enabled. Figure 4 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

SQUARE-WAVE OUTPUT FREQUENCY Figure 4

RS2	RS1	Square-Wave Output Frequency
0	0	1Hz
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

INTCN (Interrupt Control) – This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers will activate the $\overline{\text{INTA}}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers will activate the SQW/$\overline{\text{INTB}}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a match between the timekeeping registers and either alarm 1 or alarm 2 registers will activate the $\overline{\text{INTA}}$ pin (provided that the alarms are enabled). In this configuration, a square wave will be output on the SQW/$\overline{\text{INTB}}$ pin. This bit is set to logic 0 when power is first applied.

A1IE (Alarm 1 Interrupt Enable) – When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{\text{INTA}}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{\text{INTA}}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

A2IE (Alarm 2 Interrupt Enable) – When set to a logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{\text{INTA}}$ (when INTCN = 0) or to assert SQW/$\overline{\text{INTB}}$ (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

STATUS REGISTER (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

OSF (Oscillator Stop Flag) – A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit will be set to logic 1 anytime that the oscillator stops. The following are examples of conditions that may cause the OSF bit to be set:

1) The first time power is applied.
2) V_{CC} is out of tolerance.
3) The $\overline{\text{EOSC}}$ bit is turned off.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit will remain at logic 1 until written to logic 0.

A1F (Alarm 1 Flag) – A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{\text{INTA}}$ pin will go low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 will leave the value unchanged.

A2F (Alarm 2 Flag) – A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{\text{INTA}}$ pin will go low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/$\overline{\text{INTB}}$ pin will go low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 will leave the value unchanged.

2-WIRE SERIAL DATA BUS

The DS1337 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1337 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 5):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

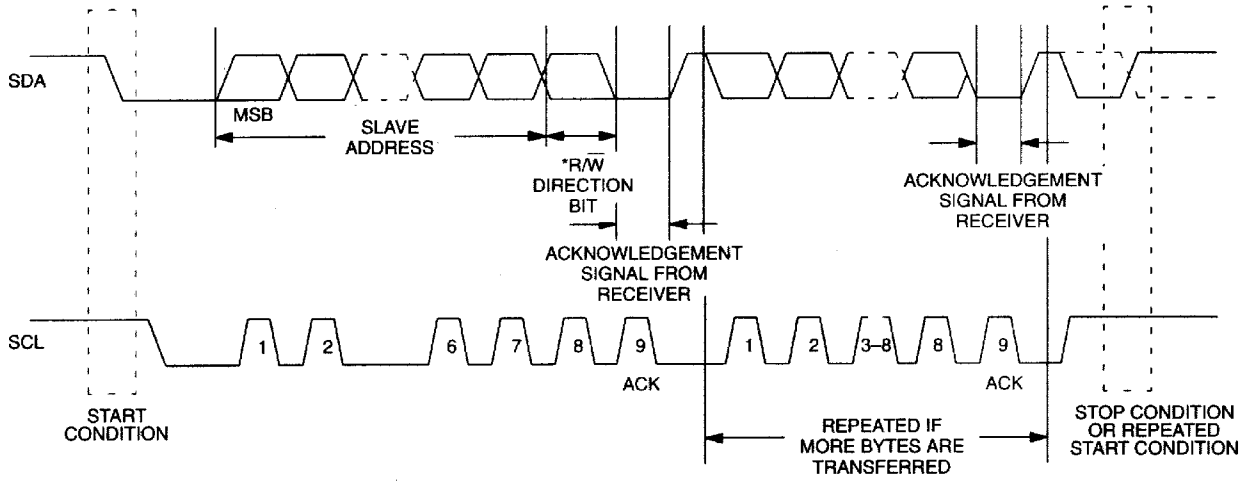
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 5



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

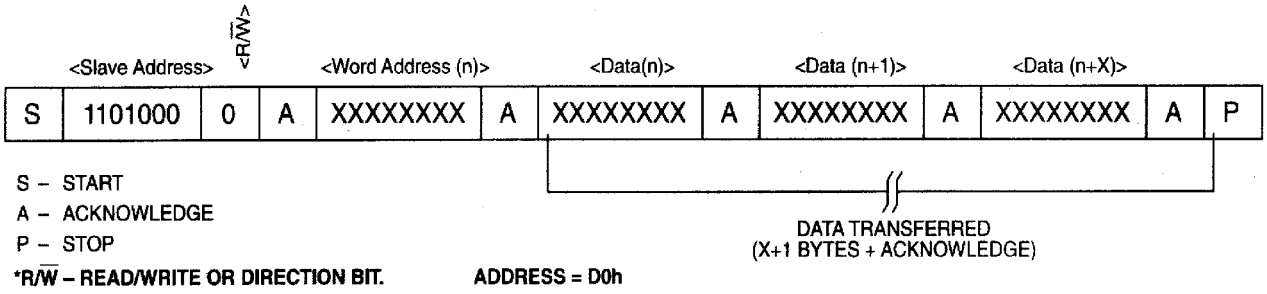
The DS1337 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 6). The slave address byte is the first byte received after the start condition is generated by the master. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$) which, for a write, is a 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the DS1337 acknowledges the slave address + write bit, the master transmits a register address to the DS1337. This will set the register pointer on the DS1337. The master will then begin transmitting each byte of data with the DS1337 acknowledging each byte received. The master will generate a stop condition to terminate the data write.

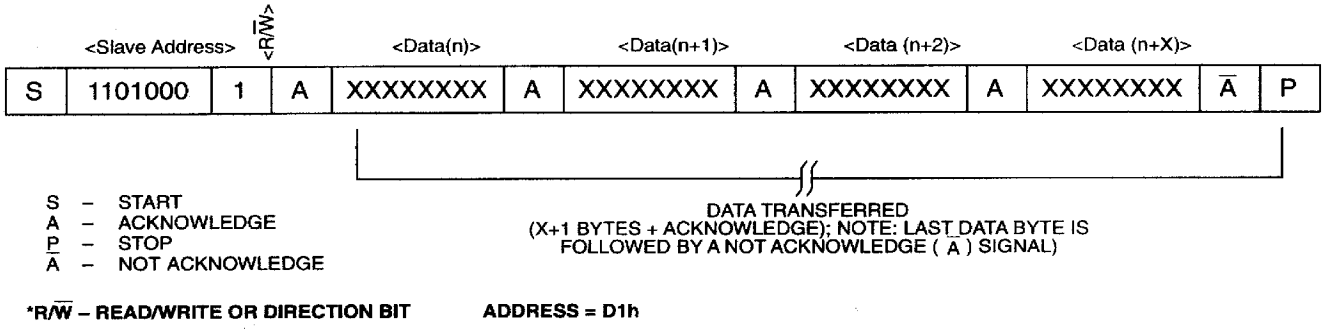
2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1337 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 7). The slave address byte is the first byte received after the start condition is generated by the master.

The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$) which, for a read, is a 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The DS1337 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1337 must receive a "not acknowledge" to end a read.

DATA WRITE—SLAVE RECEIVER MODE Figure 6



DATA READ—SLAVE TRANSMITTER MODE Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.8		4.0	V	1
Oscillator Voltage	V_{OSC}	1.3		4.0	V	1, 5
Logic 1	V_{IH}	$0.7V_{CC}$		V_{CC} + 0.5	V	1
Logic 0	V_{IL}	-0.5		$0.3V_{CC}$	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 1.8V to 4.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			1	µA	2
I/O Leakage	I_{LO}			1	µA	3
Logic 0 Output (V_{OL} = 0.4V)	I_{OL}			3	mA	3
Active Supply Current	I_{CCA}			150	µA	4
Standby Current	I_{CCS}			2	µA	5, 12

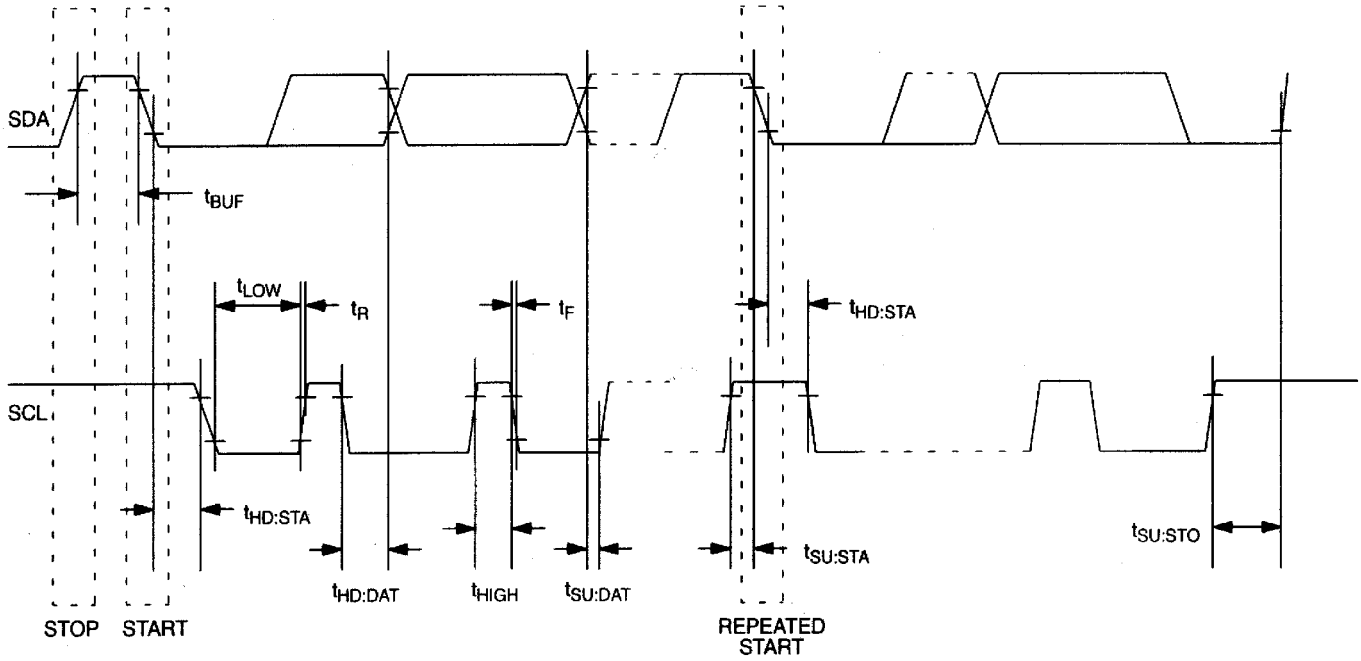
DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 1.3V to 1.8V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Timekeeping Current (Oscillator Enabled)	I_{OSC}			600	nA	5, 11
Data Retention Current (Oscillator Disabled)	I_{DDR}			50	nA	5
Crystal Specified Load Capacitance			6		pF	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 1.8V to 4.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	100		400 100	kHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	6
LOW Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
HIGH Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	7, 8
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	10
Rise Time of Both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20 + 0.1C_B$		300 1000	ns	9
Fall Time of Both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20 + 0.1C_B$		300 300	ns	9
Setup Time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive Load for Each Bus Line	C_B				400	pF	9
I/O Capacitance	$C_{I/O}$			10		pF	

TIMING DIAGRAM Figure 8



NOTES:

1. All voltages are referenced to ground.
2. SCL only.
3. SDA, $\overline{\text{INTA}}$, and SQW/$\overline{\text{INTB}}$.
4. I_{CCA}–SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}.
5. Specified with 2-wire bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}.
6. After this period, the first clock pulse is generated.
7. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
8. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
9. C_B–Total capacitance of one bus line in pF.
10. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ max} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
11. Specified with the SQW function disabled by setting INTCN = 1.
12. SQW enabled.