19-2936; Rev 0; 7/03

MAXIM

10.7Gbps Adaptive Receive Equalizer

General Description

The MAX3805 is designed to provide up to 30in (0.75m) reach on 6-mil differential FR-4 transmission line, or up to 24ft (8m) on RG-188A/U type coaxial cable, for PRBS data from 9.95Gbps to 10.7Gbps. The MAX3805 adaptive equalizer reduces intersymbol interference, resulting in 20ps residual jitter after equalization. An internal feedback network controls the equalizer to automatically match frequency-dependent skin effect and dielectric losses. The MAX3805 provides LVCMOS-compatible output-enable and signal-detect functions.

The MAX3805 has separate supply connections for the internal logic and I/O circuits. This allows the current-mode logic (CML) input and CML output to be connected to isolated supplies for independent DC-coupled interfaces to 1.8V, 2.5V, or 3.3V ICs. The MAX3805 comes in a very small 3mm x 3mm package and consumes only 135mW.

Applications

OC-192, 10GbE Switches and Routers

OC-192, 10GbE Serial Modules

High-Speed Signal Distribution

Features

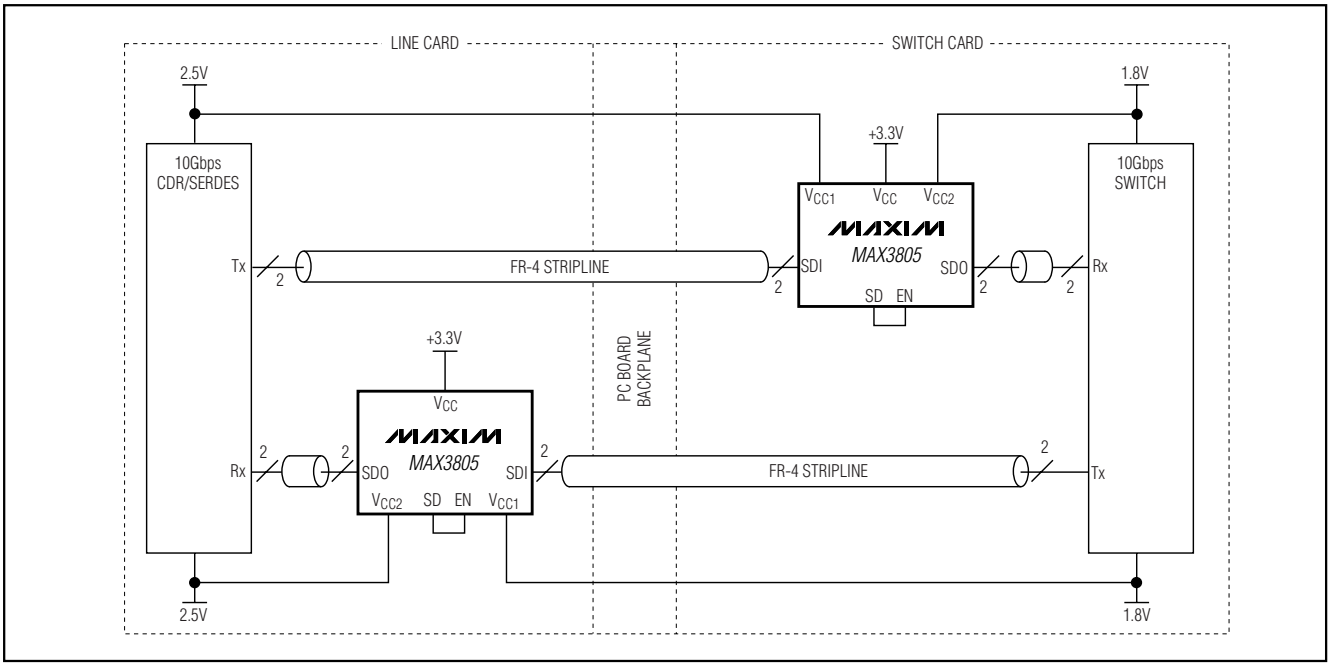
- **3mm x 3mm Package**
- **Spans 30in (0.75m) of 6-mil FR-4**
- **Spans 24ft (8m) of Coax**
- **Automatic Receive Equalization to Reduce ISI Caused by Path Losses**
- **Up to 10.7Gbps NRZ Data Operating Range**
- **Signal-Detect Output**
- **Output-Enable Control**
- **135mW Power Consumption**
- **DC-Coupled Input and Output to Terminations as Low as 1.65V**
- **Differential or Single-Ended Operation**
- **+3.3V Core Power Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3805ETE	-40°C to +85°C	16 Thin QFN	T1633F-3

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



10.7Gbps Adaptive Receive Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....-0.5V to +4.0V
CML Supply Voltage
(V_{CC1}, V_{CC2}) .....-0.5V to (V_{CC} + 0.5V)
Current at SDO± .....±25mA
SDI±, EN, SD, HFPD, LFPD.....-0.5V to (V_{CC} + 0.5V)
Current at HFPD, LFPD 400µA

Continuous Power Dissipation (T_A = +85°C)
16-Lead QFN-EP (derate 17.5mW/°C
above +85°C) 1398mW
Operating Ambient Temperature Range .....-40°C to +85°C
Storage Ambient Temperature Range.....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Input Termination Voltage	V_{CC1}		1.65		V_{CC}	V
Output Termination Voltage	V_{CC2}		1.65		V_{CC}	V
Operating Ambient Temperature			-40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

(Pin 13 (HFPD) and pin 14 (LFPD) are not connected. Typical values are at V_{CC} = +3.3V, V_{CC1} = V_{CC2} = 1.8V, T_A = +25°C, unless otherwise noted.) (Values at -40°C are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	V_{CC} = V_{CC1} = V_{CC2}		41	60	mA
CML Input Differential Voltage	V_{IN}	AC-coupled or DC-coupled at transmission line input (Notes 1, 6)	400		1200	mV_{P-P}
CML Input Common-Mode Voltage			1.3		V_{CC1}	V
CML Input Resistance		Differential	85	100	115	Ω
CML Input Return Loss		100MHz to 10GHz		10		dB
CML Output Differential Voltage	V_{OUT}	V_{CC2} = 1.65V to 3.6V	400	500	600	mV_{P-P}
CML Output Resistance		Differential	85	100	115	Ω
CML Output Transition Time	t_r/t_f	20% to 80% (Notes 2, 6)			35	ps
CML Output Return Loss		100MHz to 5GHz		10		dB
Equalizer Time Constant				10		µs
Output Residual Jitter		(Notes 3–6)		21	30	ps_{P-P}
Signal-Detect Assert		$PRBS2^{31}$ - 1 at 10.7Gbps (Note 1)		200		mV_{P-P}
Signal-Detect Deassert		$PRBS2^{31}$ - 1 at 10.7Gbps (Note 1)		220		mV_{P-P}
LVCMOS Input-High Leakage Current	I_H		+10		+60	µA

ELECTRICAL CHARACTERISTICS (continued)

(Pin 13 (HFPD) and pin 14 (LFPD) are not connected. Typical values are at V_{CC} = +3.3V, V_{CC1} = V_{CC2} = 1.8V, T_A = +25°C, unless otherwise noted.) (Values at -40°C are guaranteed by design and characterization.)

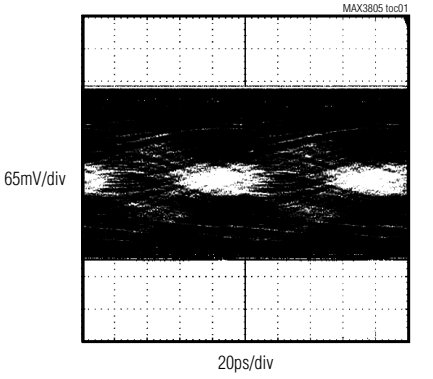
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS Input-Low Leakage Current	I_L		-30		+30	µA
LVCMOS Input High	V_{IH}		1.5			V
LVCMOS Input Low	V_{IL}				0.5	V
LVCMOS Output High	V_{OH}	I_{OH} = 12.5µA	2.1			V
LVCMOS Output Low	V_{OL}	I_{OL} = 0.5mA			0.2	V

Note 1: Differential input sensitivity is defined at the input to a transmission line with path length up to 30in.
Note 2: Measured using 10 ones and 10 zeros at 10.7Gbps.
Note 3: Residual jitter is the difference in total jitter between the signal at the input to the transmission line and the equalizer output. Total residual jitter is $DJ_{P-P} + 14.1 \times RJ_{RMS}$.
Note 4: Measured at 10.7Gbps using a pattern of 100 ones, PRBS 2^{10} - 1, 100 zeros, PRBS 2^{10} - 1.
Note 5: V_{IN} = 400mV_{P-P} to 1200mV_{P-P}, input path is 0 to 30in, 6-mil microstrip in FR-4, ε_r = 4.5, and tan δ = 0.02.
Note 6: Guaranteed by design and characterization.

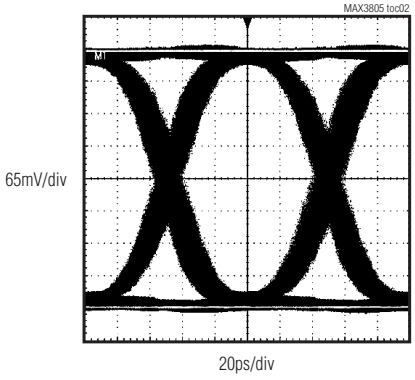
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{CC1} = 1.8V, V_{CC2} = 1.8V, and T_A = +25°C, unless otherwise noted.)

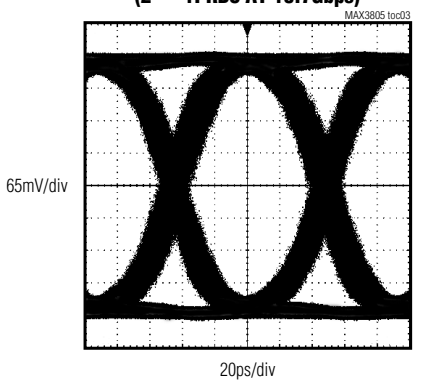
EQUALIZER INPUT EYE AFTER 30in OF FR-4 (2^{10} - 1PRBS WITH 100 CIDs AT 9.953Gbps)



EQUALIZER OUTPUT EYE AFTER 30in OF FR-4 (2^{10} - 1PRBS WITH 100 CIDs AT 9.953Gbps)



EQUALIZER OUTPUT EYE AFTER 30in OF FR-4 (2^{31} - 1PRBS AT 10.7Gbps)

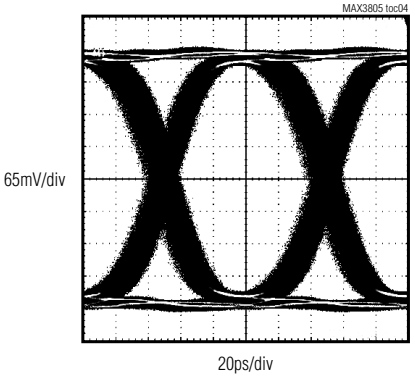


10.7Gbps Adaptive Receive Equalizer

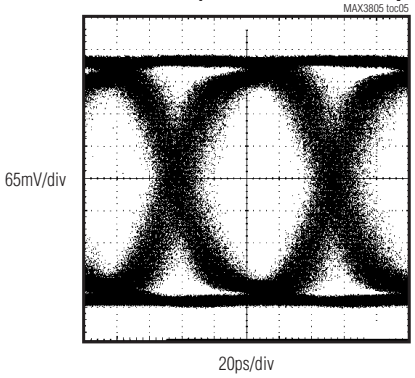
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{CC1} = 1.8V, V_{CC2} = 1.8V, and T_A = +25°C, unless otherwise noted.)

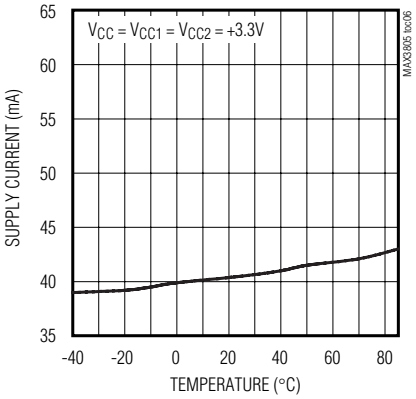
EQUALIZER OUTPUT EYE AFTER 30in OF FR-4 (CJTPAT 10.0Gbps LFPD/(HFPD + LFPD) = 0.6)



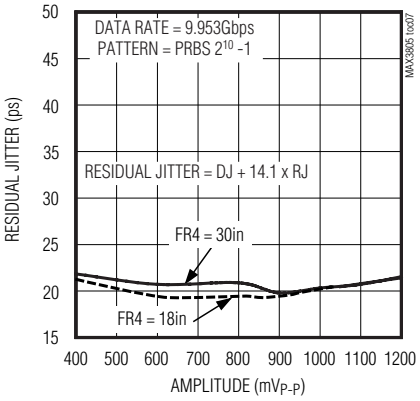
EQUALIZER OUTPUT EYE AFTER 24ft OF RG-188/U COAXIAL CABLE, SINGLE ENDED (2^{23} - 1PRBS AT 10.7Gbps)



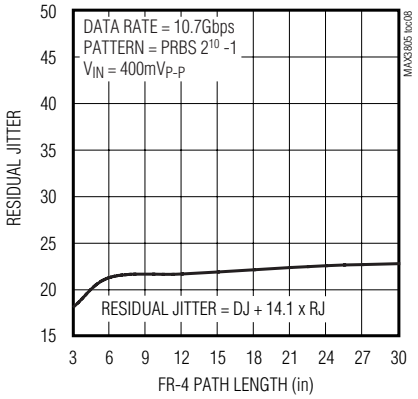
SUPPLY CURRENT vs. TEMPERATURE



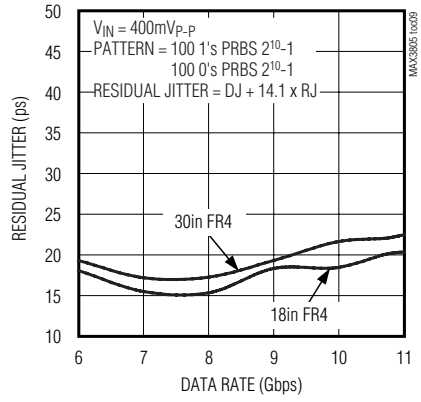
RESIDUAL JITTER vs. AMPLITUDE



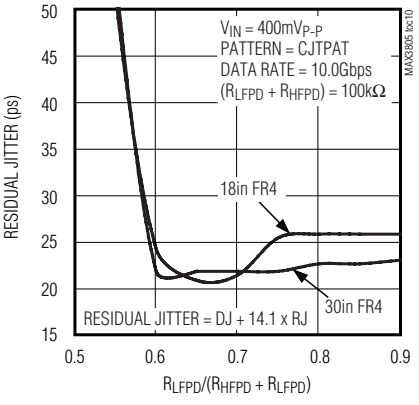
RESIDUAL JITTER vs. FR-4 PATH LENGTH



RESIDUAL JITTER vs. DATA RATE



RESIDUAL JITTER vs. $R_{LFPD}/(R_{HFPD} + R_{LFPD})$



Pin Description

PIN	NAME	FUNCTION
1	V_{CC1}	Supply Voltage, CML Input (1.8V to V_{CC})
2	SDI+	Positive Differential Serial Data Input, CML
3	SDI-	Negative Differential Serial Data Input, CML
4	V_{CC1}	Supply Voltage, CML Input (1.8V to V_{CC})
5	GND	Supply Ground
6	SD	Signal-Detect Output, LVCMOS. Low indicates <200mV_{P-P}, high indicates >220mV_{P-P}.
7	EN	Enable Input, LVCMOS. Low disables output, high enables output, typically connected to SD.
8	GND	Supply Ground
9, 12	V_{CC2}	Supply Voltage, CML Output (1.8V to V_{CC})
10	SDO-	Negative Differential Serial Data Output, CML
11	SDO+	Positive Differential Serial Data Output, CML
13	HFPD	High-Frequency Power Detector. Leave open for 9.953Gbps to 10.7Gbps PRBS NRZ data.
14	LFPD	Low-Frequency Power Detector. Leave open for 9.953Gbps to 10.7Gbps PRBS NRZ data.
15	V_{CC}	Supply Voltage, Equalizer Core, 3.3V
16	GND	Supply Ground
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground plane for proper thermal and electrical performance.

Detailed Description and Applications Information

The MAX3805 adaptive equalizer is designed to operate with 9.95Gbps to 10.7Gbps PRBS nonreturn-to-zero (NRZ) data at the receive end of a transmission line, typically differential 6-mil FR-4 PC board. It adaptively corrects intersymbol interference caused by frequency-dependent path loss. It can also be used with coaxial cable links and with transmission lines that include well-engineered connectors, as long as the total path loss is relatively smooth and does not exceed 20dB at 5GHz.

The signal path for the MAX3805 consists of a CML input stage, two amplifiers feeding a pair of variable attenuators controlled by feedback, and a limiting amplifier with a CML output stage. An enable input, EN, is used to control the output stage. A signal-detect output, SD, indicates when input signal to the transmission line is above 220mV_{P-P} or below 200mV_{P-P}, typically. See the *Functional Diagram*.

CML Input and Output Buffers

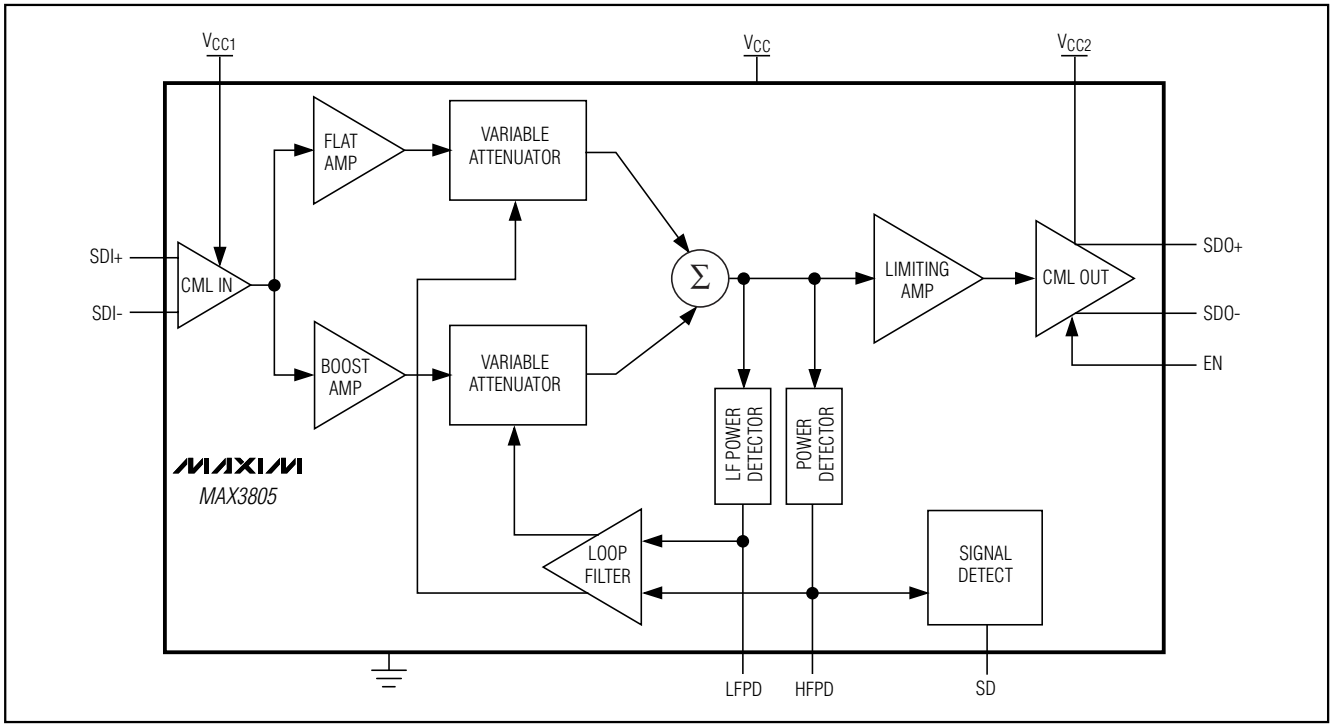
The MAX3805 CML input and output buffers are internally terminated with 50Ω to V_{CC1} and V_{CC2}, respectively. The input and output circuitry have separate voltage connections to control noise coupling and provide DC-coupling to +1.8V, +2.5V, or +3.3V CML. If desired, the CML inputs and outputs can be AC-coupled. See Figure 1 for the output structure.

The low-frequency cutoff of the input-stage offset-cancellation circuit is nominally 21kHz.

For single-ended operation (typically coaxial cable links), the input must be AC-coupled; connect the unused input to V_{CC1} using a series combination of an AC-coupling capacitor and a 50Ω resistor, as shown in Figure 2. Note that the MAX3805 is specified for differential operation, and the performance may be reduced in single-ended operation.

10.7Gbps Adaptive Receive Equalizer

Functional Diagram



Input Stage with Equalization

The low-noise input stage of the MAX3805 includes two amplifiers, one with flat frequency response and the other with a highpass frequency response compensating for the loss characteristic of 6-mil FR-4 PC board transmission line. A current-steering network, implemented with a pair of variable attenuators feeding into a common summing node, provides the means to continuously vary the amount of equalization. The amount of equalization is controlled by feedback from two power-detector blocks that set the variable attenuators to match the loss of a particular transmission path.

Dual Power-Detector Feedback Loop

The MAX3805 adapts the equalizer to a specific path loss by sampling the output of the summing node with a pair of frequency-dependent power detectors. The first power detector has a lowpass bandwidth of 500MHz; the second power detector has full bandwidth.

NRZ PRBS data has a $\sin^2(f)/f^2$ spectral characteristic. When this data is passed through a lossy FR-4 path, high-frequency components are attenuated, while low-

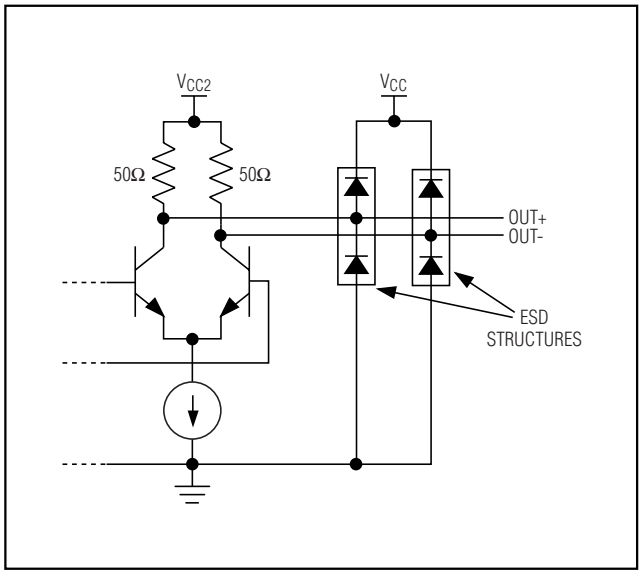


Figure 1. CML Output Structure

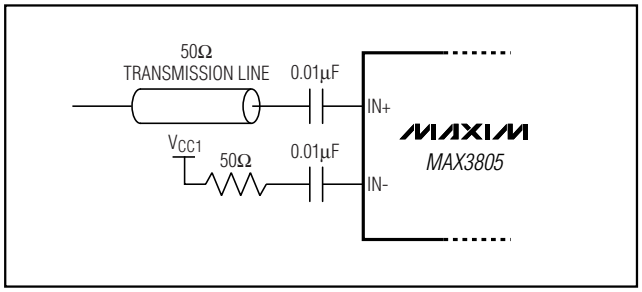


Figure 2. Single-Ended Operation

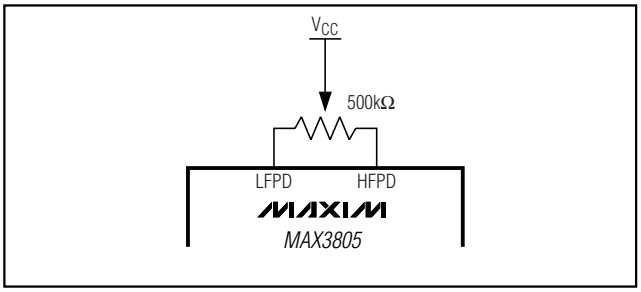


Figure 3. Connecting a Potentionmeter Across HFPD and LFPD

frequency components remain essentially intact. These changes in the spectral characteristic of the signal at the output of the path are measured with the two power detectors to provide a means to determine the path loss.

The dual power-detector feedback loop measures the ratio between the outputs of the two power detectors and adjusts the attenuation to restore the $\sin^2(f)/f^2$ characteristic. The time constant for this feedback loop is nominally 10µs.

Operating with Different Data Rates and Codes

The MAX3805 equalizer feedback loop is optimized for 9.95Gbps to 10.7Gbps NRZ PRBS data; however, it can also be used at a lower data rate or with a different coding type by adjusting the feedback loop. The relative gain of the two power detectors can be adjusted by connecting a 500kΩ trimmer potentiometer between HFPD and LFPD pins, with the wiper connected to V_{CC}, as shown in Figure 3. Set the trimmer potentiometer for the best eye opening.

Adding the potentiometer between HFPD and LFPD can change the assert and deassert levels of the signal detector, which could render the signal-detect output invalid. For normal operation with 9.953Gbps to 10.7Gbps PRBS NRZ data, these signals should be left open with no connections to pin 13 (HFPD) or pin 14 (LFPD). Note that excessive capacitance on pin 13 or pin 14 can affect the operation of the feedback loop. Make certain that the PC board traces from these pins to the trimmer potentiometer are kept short.

Enable Function

The EN output is an LVCMOS-compatible pin that enables the output stage of the MAX3805. Connect EN to V_{CC} or LVCMOS high to enable the output stage of the device or to GND or LVCMOS low to disable the output stage of the device.

Signal Detect

The output of the high-frequency power detector is used to generate an LVCMOS-compatible signal-detect (SD) output. The SD output asserts when the input signal at the transmission line falls below $200mV_{P-P}$, and deasserts when the input signal at the transmission line rises above $220mV_{P-P}$. The SD output can be directly connected to the EN input to disable the MAX3805 output when no data signal is available. The SD output has an LVCMOS fanout of one.

Package and Layout Considerations

The MAX3805 is packaged in a 3mm x 3mm plastic-encapsulated 16-lead thin QFN package with exposed pad for signal integrity. The exposed pad provides thermal and electrical connectivity to the IC, and must be soldered to a high-frequency ground plane. Use good layout techniques for the10Gbps SDI and SDO PC board transmission lines, and configure the trace geometry near the IC package to minimize impedance discontinuities. Power-supply decoupling capacitors should be provided for each supply connection and located as close as practical to the IC package.

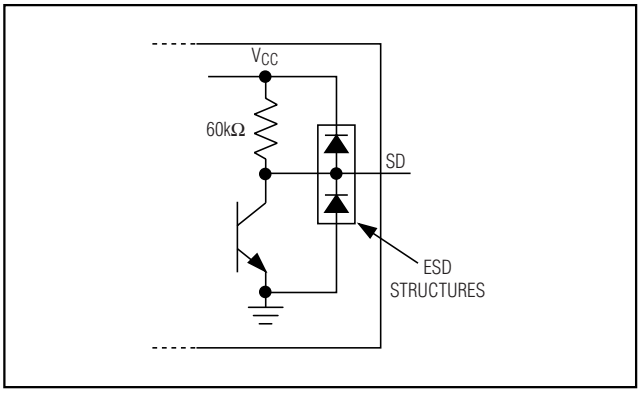


Figure 4. Signal-Detect Output Circuit

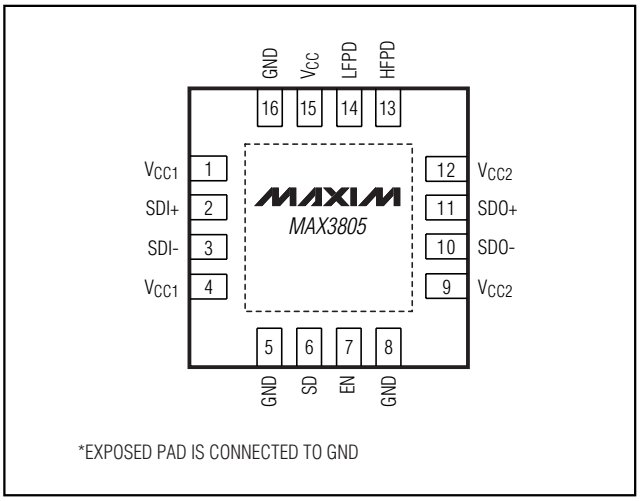
10.7Gbps Adaptive Receive Equalizer

Chip Information

TRANSISTOR COUNT: 1647

PROCESS: SiGe Bipolar

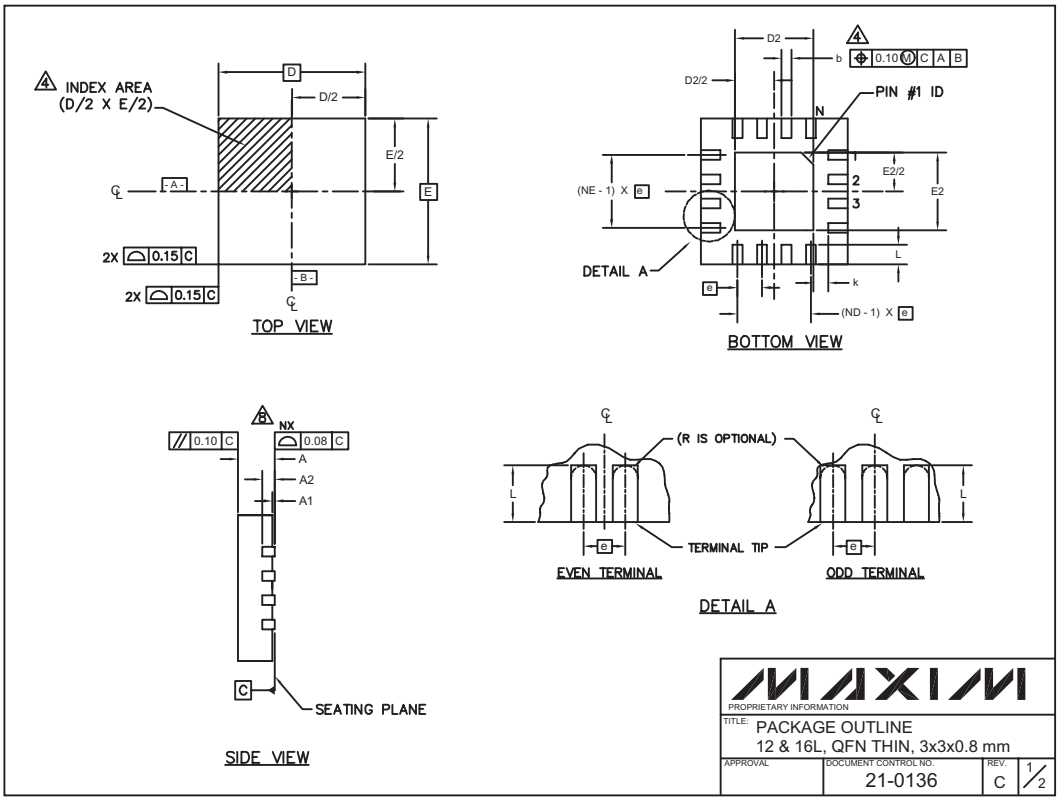
Pin Configuration



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



10.7Gbps Adaptive Receive Equalizer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12 & 16L, QFN THIN, 3x3x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. C	2/2