19-1172; Rev 0; 12/96

# +3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

MAX5251

## General Description

The +3V MAX5251 combines four low-power, voltage-output, 10-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX5251 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset that clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. All logic inputs are TTL/CMOS-logic compatible.

## Applications

- Digital Offset and Gain Adjustment
- Microprocessor-Controlled Systems
- Industrial Process Controls
- Automatic Test Equipment
- Remote Industrial Controls
- Motion Control

## Features

- ♦ **Four 10-Bit DACs with Configurable Output Amplifiers**
- ♦ **+3.0V to +3.6V Single-Supply Operation**
- ♦ **Low Supply Current: 0.8mA Normal Operation 3µA Shutdown Mode**
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- ♦ **12-Bit Upgrade Available: MAX5253**

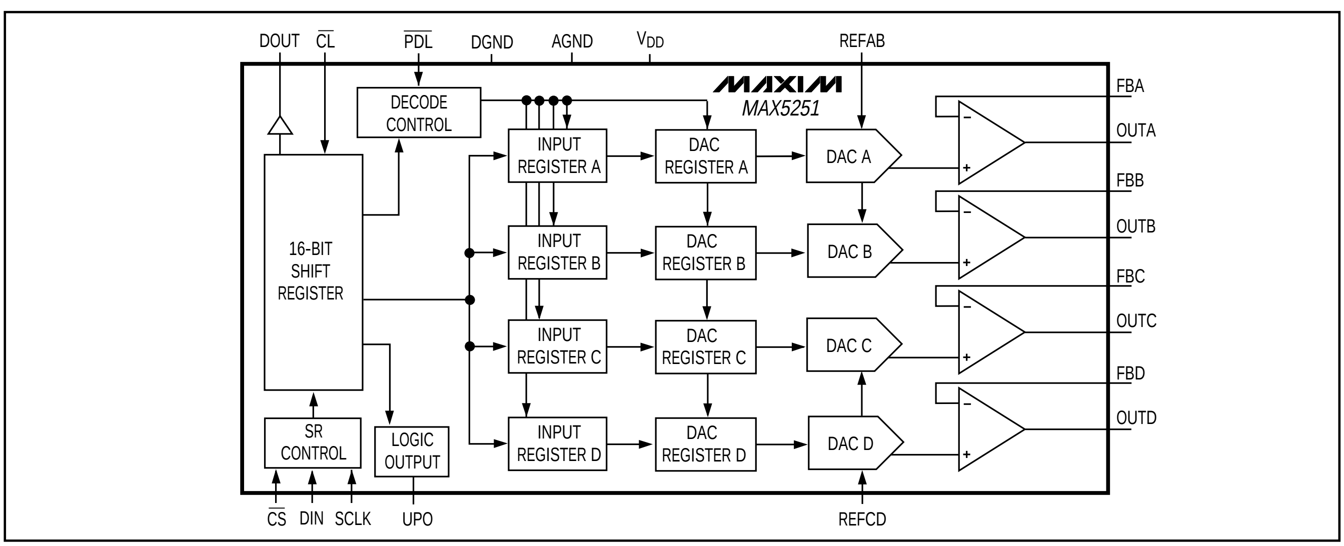
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | INL (LSB) |
|---|---|---|---|
| MAX5251ACPP | 0°C to +70°C | 20 Plastic DIP | ±1/2 |
| MAX5251BCPP | 0°C to +70°C | 20 Plastic DIP | ±1 |
| MAX5251ACAP | 0°C to +70°C | 20 SSOP | ±1/2 |
| MAX5251BCAP | 0°C to +70°C | 20 SSOP | ±1 |

***Ordering Information continued on last page.***

***Pin Configuration appears at end of data sheet.***

## Functional Diagram

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## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND ............ -0.3V to +6V
$V_{DD}$ to DGND ............ -0.3V to +6V
AGND to DGND ............ ±0.3V
REFAB, REFCD to AGND ............ -0.3V to ($V_{DD}$ + 0.3V)
OUT_, FB_ to AGND ............ -0.3V to ($V_{DD}$ + 0.3V)
Digital Inputs to DGND ............ -0.3V to +6V
DOUT, UPO to DGND ............ -0.3V to ($V_{DD}$ + 0.3V)
Continuous Current into Any Pin ............ ±20mA
Continuous Power Dissipation ($T_A$ = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) ............ 640mW
SSOP (derate 8.00mW/°C above +70°C) ............ 640mW
CERDIP (derate 11.11mW/°C above +70°C) ............ 889mW

Operating Temperature Ranges
MAX5251_C_P ............ 0°C to +70°C
MAX5251_E_P ............ -40°C to +85°C
MAX5251BMJP ............ -55°C to +125°C
Storage Temperature Range ............ -65°C to +150°C
Lead Temperature (soldering, 10sec) ............ +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE—ANALOG SECTION** | | | | | | |
| Resolution | N | | 10 | | | Bits |
| Integral Nonlinearity (Note 1) | INL | MAX5251AC/E | | ±0.25 | ±0.5 | LSB |
| | | MAX5251BC/E | | | ±1.0 | |
| | | MAX5251BMJP | | | ±2.0 | |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | ±1.0 | LSB |
| Offset Error | $V_{OS}$ | | | | ±6.0 | mV |
| Offset-Error Tempco | | | | 6 | | ppm/°C |
| Gain Error (Note 1) | GE | | | | ±2.4 | LSB |
| Gain-Error Tempco | | | | 1 | | ppm/°C |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = +3.0V to +3.6V | | 100 | 800 | µV/V |
| **REFERENCE INPUT** | | | | | | |
| Reference Input Range | $V_{REF}$ | | 0 | | $V_{DD}$ - 1.4 | V |
| Reference Input Resistance | $R_{REF}$ | Code dependent, minimum at code 554 hex | 10 | | | kΩ |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **MULTIPLYING-MODE PERFORMANCE** | | | | | | |
| Reference -3dB Bandwidth | | $V_{REF}$ = 0.67Vp-p | | 650 | | kHz |
| Reference Feedthrough | | Input code = all 0s, $V_{REF}$ = 1.6Vp-p at 1kHz | | -84 | | dB |
| Signal-to-Noise Plus Distortion Ratio | SINAD | $V_{REF}$ = 1Vp-p at 25kHz, code = full scale | | 72 | | dB |
| **DIGITAL INPUTS** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2.0 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.6 | V |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 0V or $V_{DD}$ | | 0.01 | ±1.0 | µA |
| Input Capacitance | $C_{IN}$ | | | 8 | | pF |
| **DIGITAL OUTPUTS** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 2mA | $V_{DD}$ - 0.5 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 2mA | | 0.13 | 0.4 | V |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Voltage Output Slew Rate | SR | | | 0.6 | | V/µs |
| Output Settling Time | | To ±1/2LSB, $V_{STEP}$ = 1.25V | | 12 | | µs |
| Output Voltage Swing | | Rail-to-rail (Note 2) | | 0 to $V_{DD}$ | | V |
| Current into FB_ | | | | 0 | 0.1 | µA |
| OUT_ Leakage Current in Shutdown | | $R_L$ = ∞ | | 0.01 | ±1 | µA |
| Start-Up Time Exiting Shutdown Mode | | | | 20 | | µs |
| Digital Feedthrough | | $\overline{CS}$ = $V_{DD}$, DIN = 100kHz | | 5 | | nV-s |
| Digital Crosstalk | | | | 5 | | nV-s |
| **POWER SUPPLIES** | | | | | | |
| Supply Voltage | $V_{DD}$ | (Note 3) | 3.0 | | 3.6 | V |
| Supply Current | $I_{DD}$ | (Note 4) | | 0.82 | 0.98 | mA |
| Supply Current in Shutdown | | (Note 4) | | 3 | 20 | µA |
| Reference Current in Shutdown | | | | 0.01 | ±1 | µA |

**Note 1:** Guaranteed from code 5 to code 1023 in unity-gain configuration.
**Note 2:** Accuracy is better than 1LSB for $V_{OUT}$ = 6mV to $V_{DD}$ - 80mV, guaranteed by PSR test at the endpoints.
**Note 3:** Remains operational with supply voltage as low as +2.7V.
**Note 4:** $R_L$ = ∞, digital inputs at DGND or $V_{DD}$.

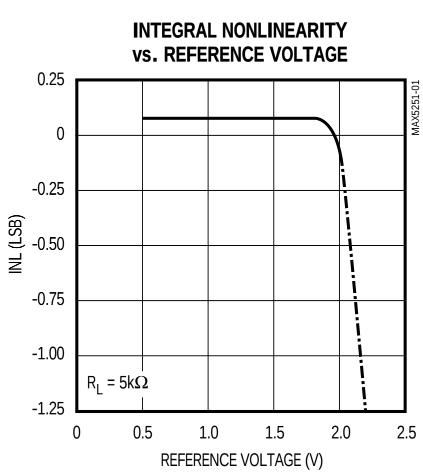
## ELECTRICAL CHARACTERISTICS (continued)

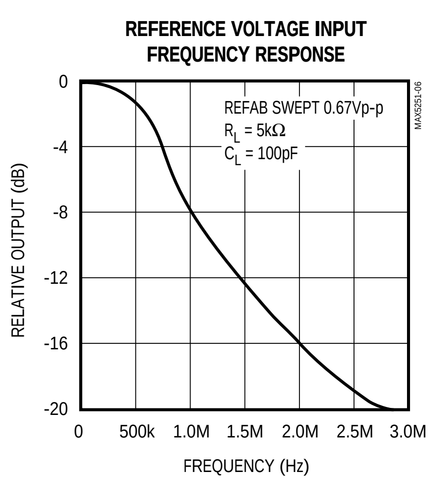
($V_{DD}$ = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

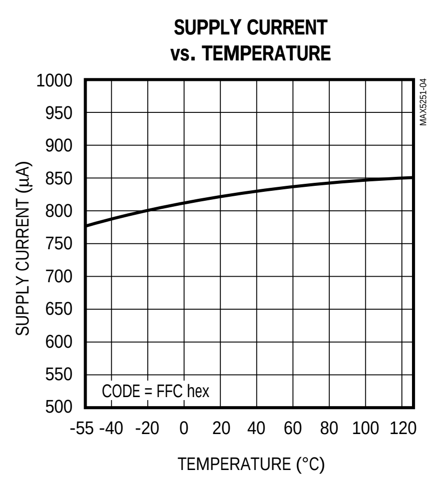
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS** (Figure 6) | | | | | | |
| SCLK Clock Period | $t_{CP}$ | | 100 | | | ns |
| SCLK Pulse Width High | $t_{CH}$ | | 40 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | | 40 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$ | | 40 | | | ns |
| SCLK Rise to $\overline{CS}$ Rise Hold Time | $t_{CSH}$ | | 0 | | | ns |
| DIN Setup Time | $t_{DS}$ | | 40 | | | ns |
| DIN Hold Time | $t_{DH}$ | | 0 | | | ns |
| SCLK Rise to DOUT Valid Propagation Delay | $t_{D01}$ | $C_L$ = 200pF | | | 120 | ns |
| SCLK Fall to DOUT Valid Propagation Delay | $t_{D02}$ | $C_L$ = 200pF | | | 120 | ns |
| SCLK Rise to $\overline{CS}$ Fall Delay | $t_{CS0}$ | | 40 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Hold Time | $t_{CS1}$ | | 40 | | | ns |
| $\overline{CS}$ Pulse Width High | $t_{CSW}$ | | 100 | | | ns |

## Typical Operating Characteristics

($V_{DD}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

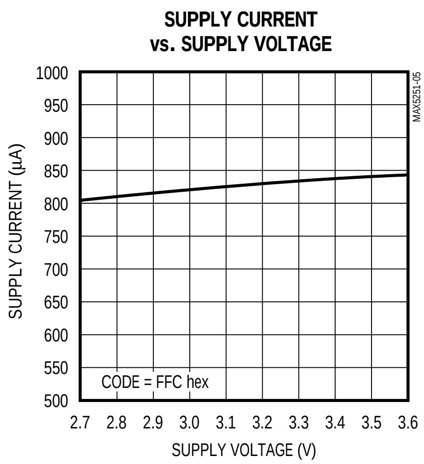


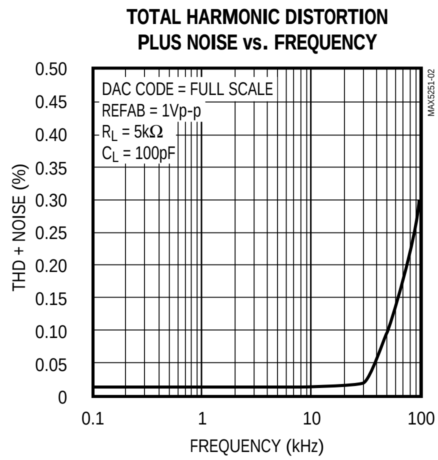



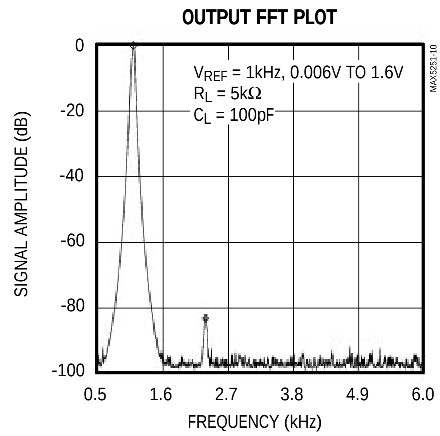



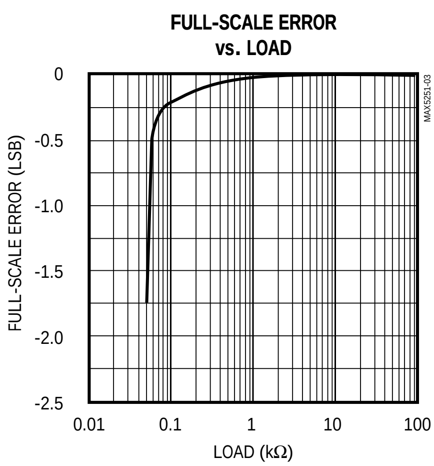
## Typical Operating Characteristics (continued)

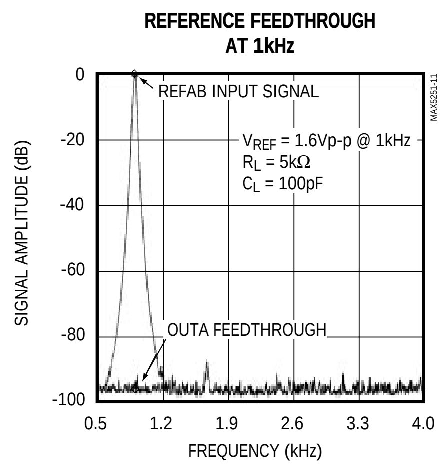
($V_{DD}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)



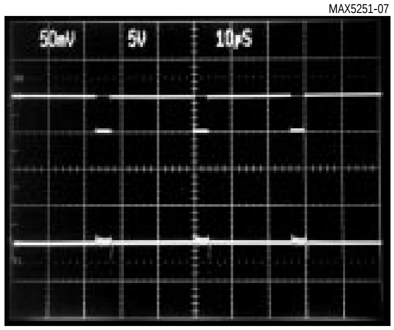



## Typical Operating Characteristics (continued)

($V_{DD}$ = +3.3V, $V_{REF}$ = 1.25V, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

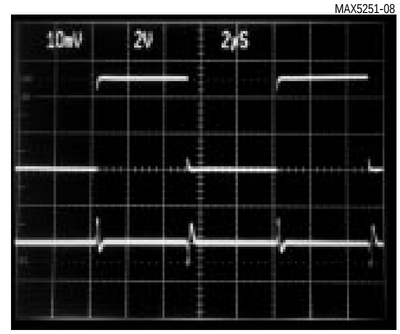
**MAJOR-CARRY TRANSITION**

MAX5251-07




**DIGITAL FEEDTHROUGH (SCLK = 100kHz)**

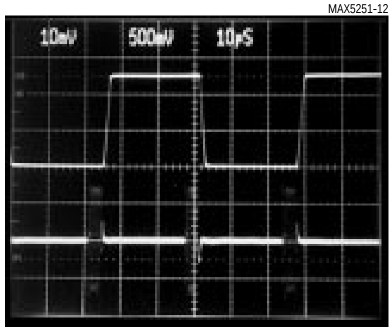
MAX5251-08




$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 3.3V, DIN = 0V
DAC A CODE SET TO 800 hex

**ANALOG CROSSTALK**

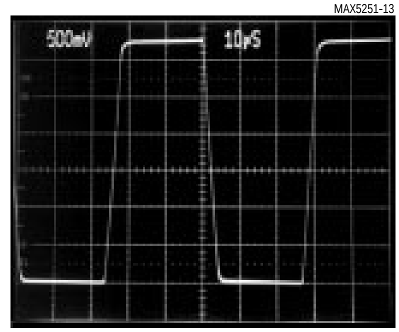
MAX5251-12




DAC A CODE SWITCHING FROM 00C hex TO FFC hex
DAC B CODE SET TO 800 hex

**DYNAMIC RESPONSE**

MAX5251-13




SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2.6

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | AGND | Analog Ground |
| 2 | FBA | DAC A Output Amplifier Feedback |
| 3 | OUTA | DAC A Output Voltage |
| 4 | OUTB | DAC B Output Voltage |
| 5 | FBB | DAC B Output Amplifier Feedback |
| 6 | REFAB | Reference Voltage Input for DAC A and DAC B |
| 7 | $\overline{CL}$ | Clears All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low. |
| 8 | $\overline{CS}$ | Chip-Select Input. Active low. |
| 9 | DIN | Serial-Data Input |
| 10 | SCLK | Serial-Clock Input |
| 11 | DGND | Digital Ground |
| 12 | DOUT | Serial-Data Output |
| 13 | UPO | User-Programmable Logic Output |
| 14 | $\overline{PDL}$ | Power-Down Lockout. Active low. Locks out software shutdown if low. |
| 15 | REFCD | Reference Voltage Input for DAC C and DAC D |
| 16 | FBC | DAC C Output Amplifier Feedback |
| 17 | OUTC | DAC C Output Voltage |
| 18 | OUTD | DAC D Output Voltage |
| 19 | FBD | DAC D Output Amplifier Feedback |
| 20 | $V_{DD}$ | Positive Power Supply |

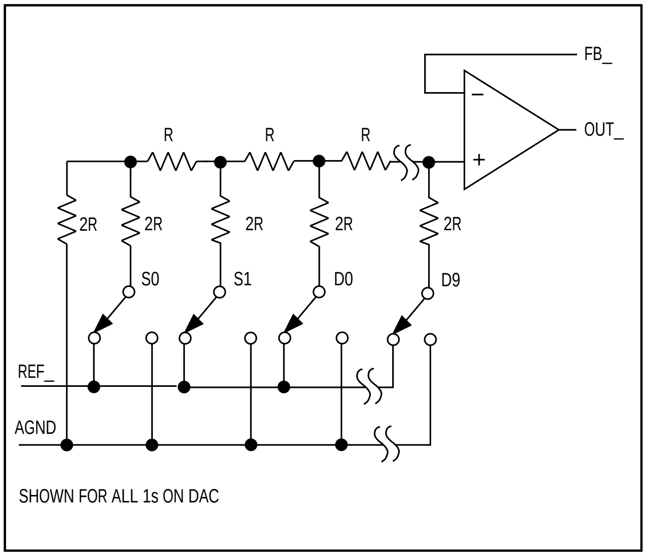



*Figure 1. Simplified DAC Circuit Diagram*

## Detailed Description

The MAX5251 contains four voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert a digital input (10 data bits plus 2 sub-bits) into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

### Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to ($V_{DD}$ - 1.4V). The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times NB / 1024) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 1023), $V_{REF}$ is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 554 hex, to a high value exceeding several giga ohms (leakage current) with an input code of 000 hex. Because the input impedance at the reference pins is code dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX5251's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF at full scale.

### Output Amplifiers

All MAX5251 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to each output amplifier's inverting input provides the user greater flexibility in output gain setting/ signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5251 output, the typical settling time to ±1/2LSB is 12µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX5251 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

### Power-Down Mode

The MAX5251 features a software-programmable shutdown that reduces supply current to a typical value of 3µA. The power-down lockout pin ($\overline{PDL}$) must be high to enable shutdown mode. Writing 1100XXXXXXXXXXXX as the input-control word puts the MAX5251 in shutdown mode (Table 1).

In shutdown mode, the MAX5251 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX5251 to recall the output states prior to entering shutdown. Exit shutdown mode either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the outputs to stabilize.

### *Serial-Interface Configurations*

The MAX5251's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 10+2 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX5251's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX5251's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX5251's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

### *Serial-Interface Description*

The MAX5251 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 10+2 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 10+2 data bits D9…D0, S1, S0 (Figure 4). Set both sub-bits (S0, S1) to zero. The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when exiting shutdown mode.

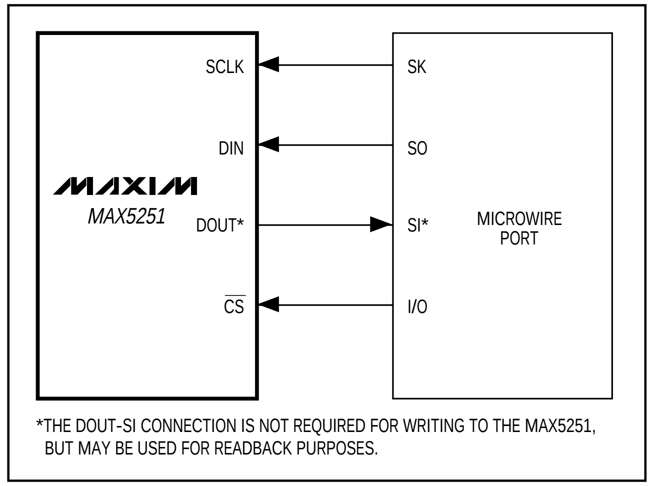



*Figure 2. Connections for Microwire*

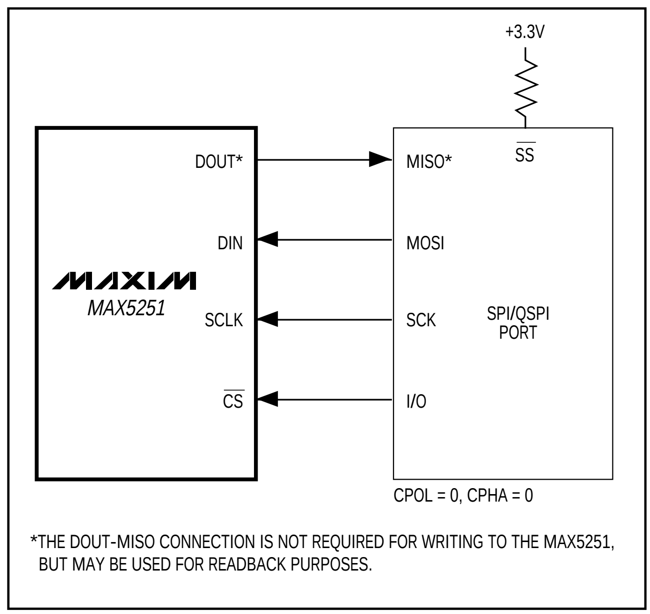



*Figure 3. Connections for SPI/QSPI*

| MSB ........................................LSB | | |
|---|---|---|
| ← 16 Bits of Serial Data → | | |
| Address Bits | Control Bits | Data Bits MSB..........LSB |
| A1 A0 | C1 C0 | D9 ..........D0 S1 S0 |
| ← 4 Address/Control Bits → | | ← 10+2 Data Bits → |

*Figure 4. Serial-Data Format*

## Table 1. Serial-Interface Programming Commands

| 16-BIT SERIAL WORD | | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|
| A1 | A0 | C1 | C0 | D9................D0 MSB............LSB | S1 | S0 | |
| 0 | 0 | 0 | 1 | 10-bit DAC data | 0 | 0 | Load input register A; DAC registers unchanged. |
| 0 | 1 | 0 | 1 | 10-bit DAC data | 0 | 0 | Load input register B; DAC registers unchanged. |
| 1 | 0 | 0 | 1 | 10-bit DAC data | 0 | 0 | Load input register C; DAC registers unchanged. |
| 1 | 1 | 0 | 1 | 10-bit DAC data | 0 | 0 | Load input register D; DAC registers unchanged. |
| 0 | 0 | 1 | 1 | 10-bit DAC data | 0 | 0 | Load input register A; all DAC registers updated. |
| 0 | 1 | 1 | 1 | 10-bit DAC data | 0 | 0 | Load input register B; all DAC registers updated. |
| 1 | 0 | 1 | 1 | 10-bit DAC data | 0 | 0 | Load input register C; all DAC registers updated. |
| 1 | 1 | 1 | 1 | 10-bit DAC data | 0 | 0 | Load input register D; all DAC registers updated. |
| 0 | 1 | 0 | 0 | XXXXXXXXXX | X | X | Update all DAC registers from their respective input registers (also exit shutdown mode). |
| 1 | 0 | 0 | 0 | 10-bit DAC data | 0 | 0 | Load all DAC registers from shift register (also exit shutdown mode). |
| 1 | 1 | 0 | 0 | XXXXXXXXXX | X | X | Enter shutdown mode (provided $\overline{PDL}$ = 1). |
| 0 | 0 | 1 | 0 | XXXXXXXXXX | X | X | UPO goes low (default). |
| 0 | 1 | 1 | 0 | XXXXXXXXXX | X | X | UPO goes high. |
| 0 | 0 | 0 | 0 | XXXXXXXXXX | X | X | No operation (NOP) to DAC registers |
| 1 | 1 | 1 | 0 | XXXXXXXXXX | X | X | Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated. |
| 1 | 0 | 1 | 0 | XXXXXXXXXX | X | X | Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default). |

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least $t_{CSS}$ before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX5251 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX5251 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

### *Serial-Data Output (DOUT)*

The serial-data output, DOUT, is the internal shift register's output. The MAX5251 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

### *User-Programmable Logic Output (UPO)*

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX5251 serial interface (Table 1).

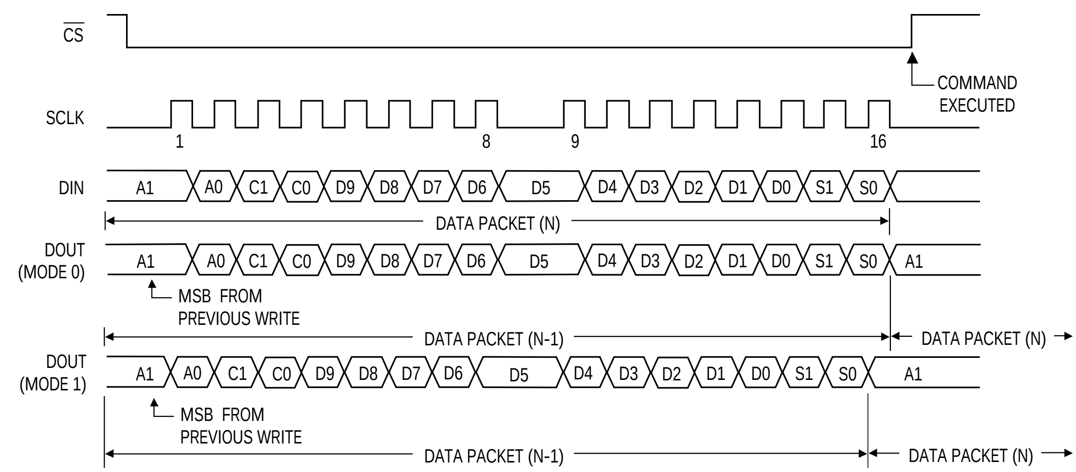



*Figure 5. Serial-Interface Timing Diagram*

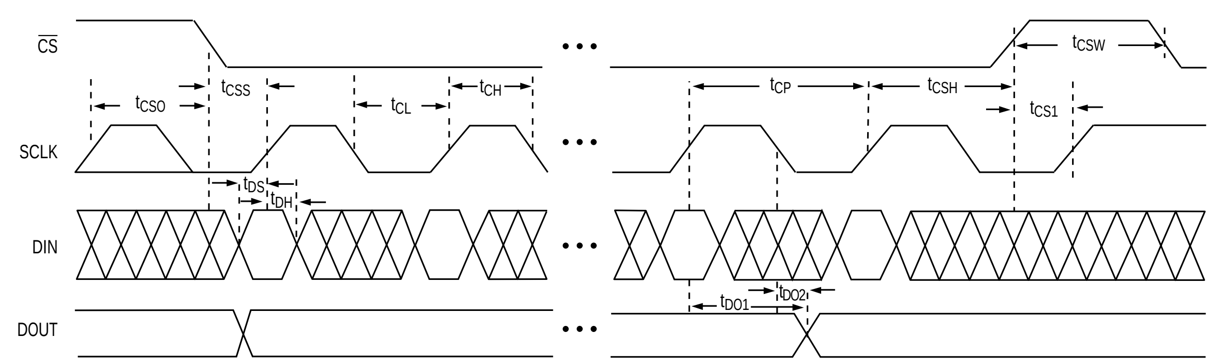



*Figure 6. Detailed Serial-Interface Timing Diagram*

### *Power-Down Lockout ($\overline{\textbf{PDL}}$)*

The power-down lockout pin $\overline{PDL}$ disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ could also be used to wake up the device asynchronously.

### *Daisy Chaining Devices*

Any number of MAX5251s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5251's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out $V_{OH}$ and $V_{OL}$ specifications in the *Electrical Characteristics.*

Figure 8 shows an alternate method of connecting several MAX5251s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

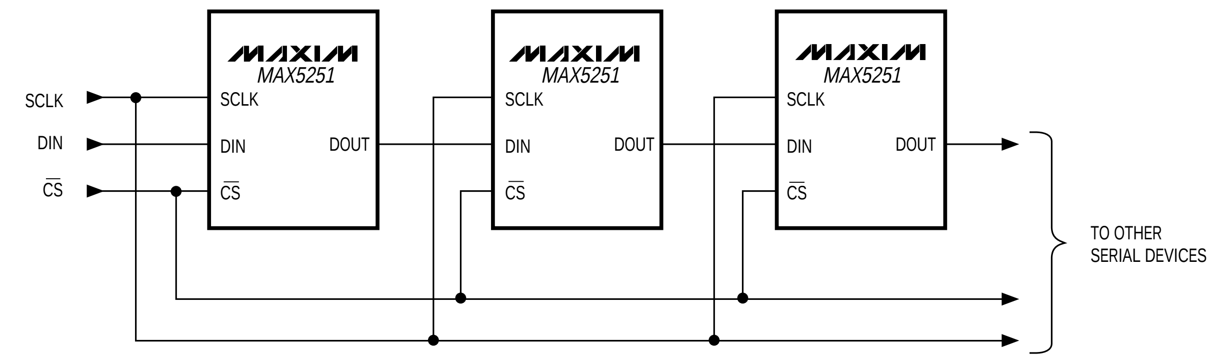



*Figure 7. Daisy-Chaining MAX5251s*

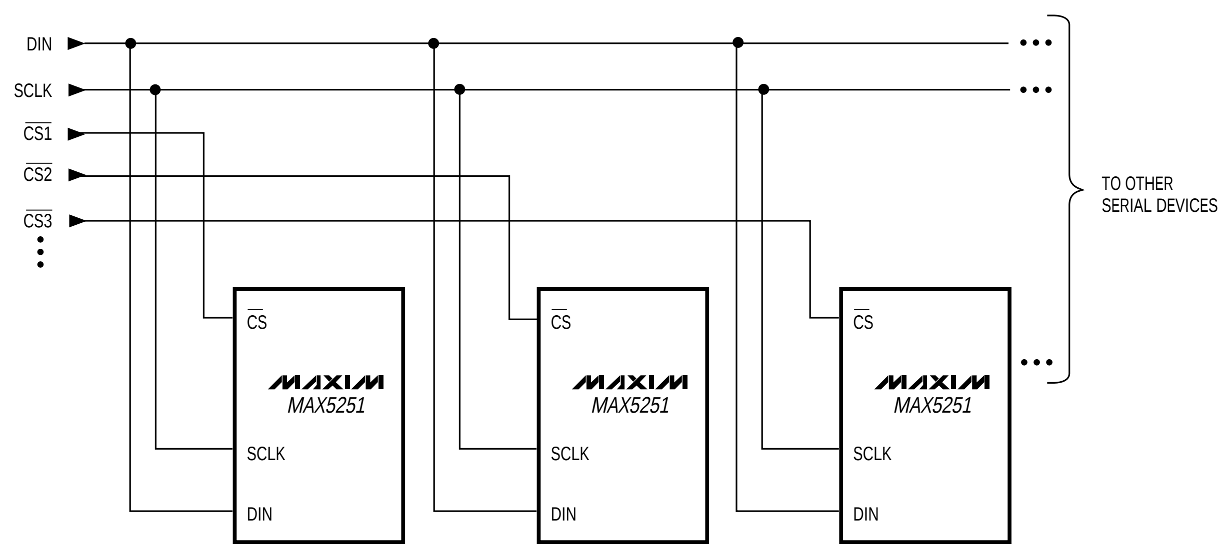



*Figure 8. Multiple MAX5251s Sharing a Common DIN Line*

## Applications Information

### Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX5251 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX5251 with the output amplifiers configured with a closed-loop gain of +2.6 to provide 0V to 3.25V full-scale range when a 1.25V reference is used.

### Table 2. Unipolar Code Table

| DAC CONTENTS MSB | | LSB | ANALOG OUTPUT |
|---|---|---|---|
| 1111 | 1111 | 11(00) | $+V_{REF}\left(\frac{1023}{1024}\right)$ |
| 1000 | 0000 | 01(00) | $+V_{REF}\left(\frac{513}{1024}\right)$ |
| 1000 | 0000 | 00(00) | $+V_{REF}\left(\frac{512}{1024}\right) = \frac{+V_{REF}}{2}$ |
| 0111 | 1111 | 11(00) | $+V_{REF}\left(\frac{511}{1024}\right)$ |
| 0000 | 0000 | 01(00) | $+V_{REF}\left(\frac{1}{1024}\right)$ |
| 0000 | 0000 | 00(00) | 0V |

### Table 3. Bipolar Code Table

| DAC CONTENTS MSB | | LSB | ANALOG OUTPUT |
|---|---|---|---|
| 1111 | 1111 | 11(00) | $+V_{REF}\left(\frac{511}{512}\right)$ |
| 1000 | 0000 | 01(00) | $+V_{REF}\left(\frac{1}{512}\right)$ |
| 1000 | 0000 | 00(00) | 0V |
| 0111 | 1111 | 11(00) | $-V_{REF}\left(\frac{1}{512}\right)$ |
| 0000 | 0000 | 01(00) | $-V_{REF}\left(\frac{511}{512}\right)$ |
| 0000 | 0000 | 00(00) | $-V_{REF}\left(\frac{512}{512}\right) = -V_{REF}$ |

( ) Sub-bits

### Bipolar Output

The MAX5251 outputs can be configured for bipolar operation using Figure 11's circuit:

$$V_{OUT} = V_{REF}\,[(2NB / 1024) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

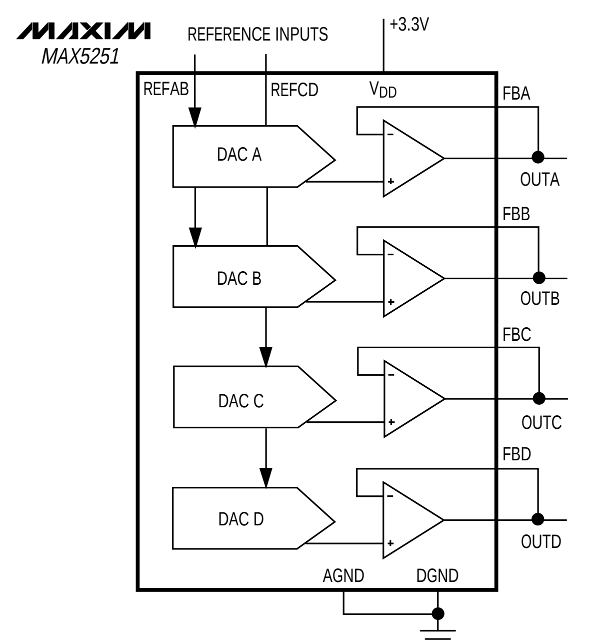



*Figure 9. Unipolar Output Circuit*

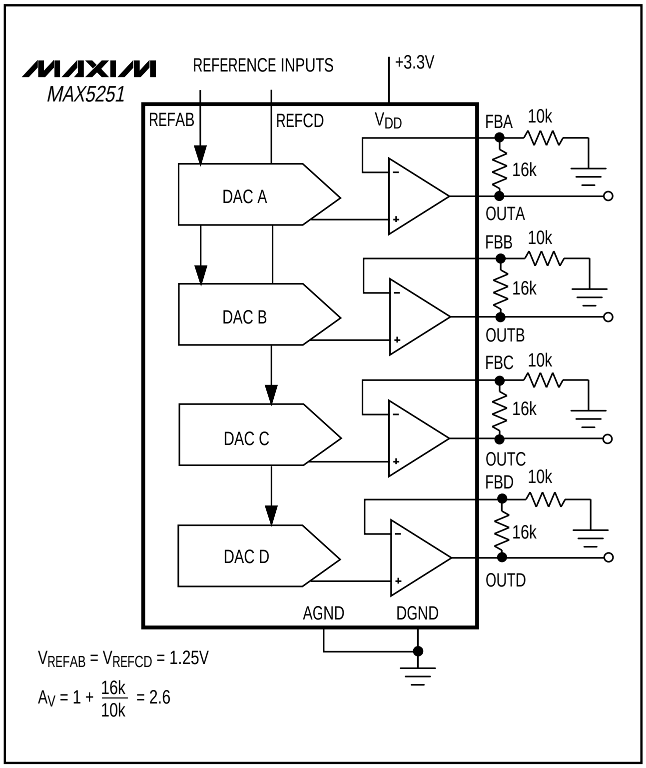



*Figure 10. Unipolar Rail-to-Rail Output Circuit*

### *Using an AC Reference*

In applications where the reference has AC signal components, the MAX5251 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX5251's total harmonic distortion plus noise (THD + N) is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

### *Digitally Programmable Current Source*

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4–20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 1024)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

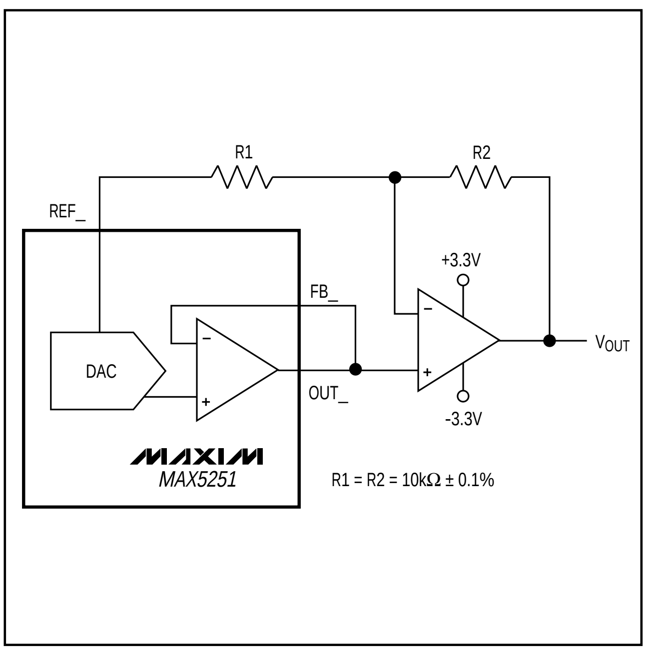



*Figure 11. Bipolar Output Circuit*

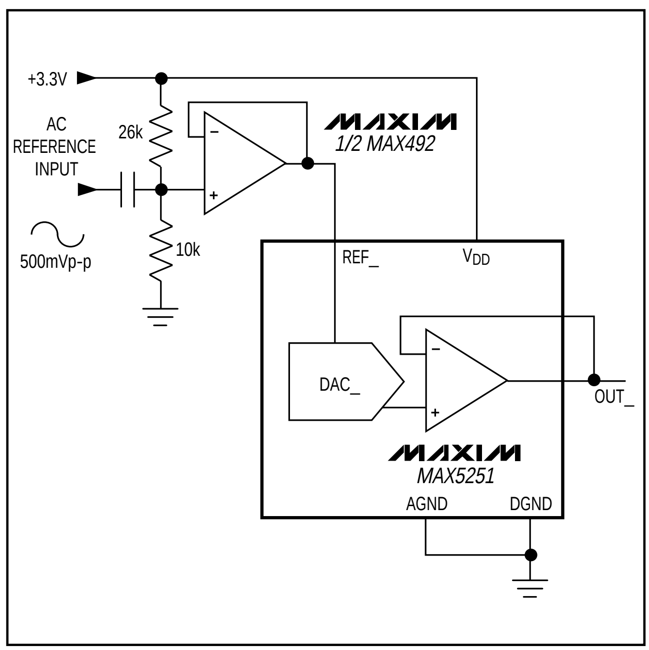



*Figure 12. AC Reference Input Circuit*

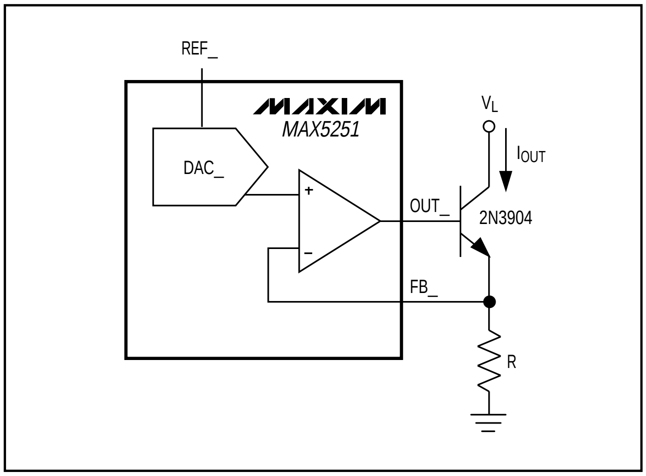



*Figure 13. Digitally Programmable Current Source*

### Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

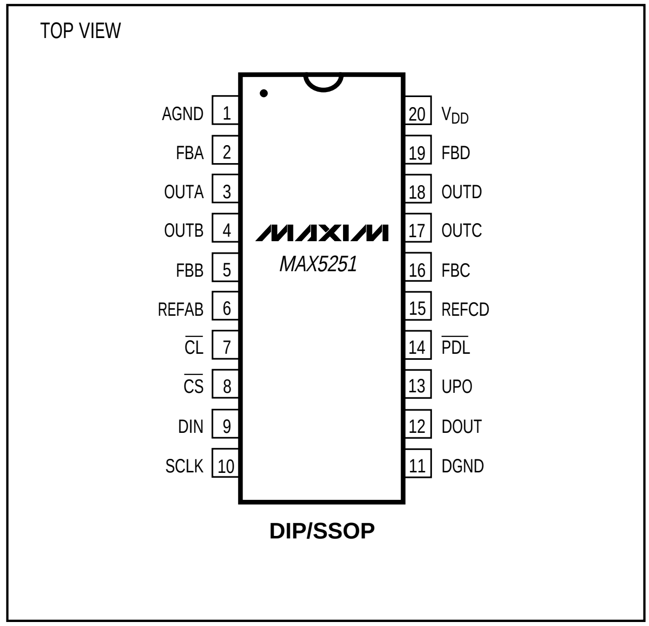
For rated MAX5251 performance, limit REFAB/REFCD to less than 1.4V below $V_{DD}$. Bypass $V_{DD}$ with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

### Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

## Pin Configuration



## Ordering Information (continued)

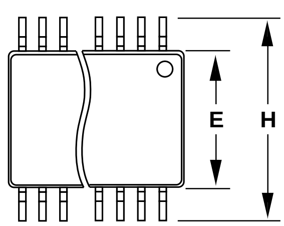
| PART | TEMP. RANGE | PIN-PACKAGE | INL (LSB) |
|---|---|---|---|
| MAX5251AEPP | -40°C to +85°C | 20 Plastic DIP | ±1/2 |
| MAX5251BEPP | -40°C to +85°C | 20 Plastic DIP | ±1 |
| MAX5251AEAP | -40°C to +85°C | 20 SSOP | ±1/2 |
| MAX5251BEAP | -40°C to +85°C | 20 SSOP | ±1 |
| MAX5251BMJP | -55°C to +125°C | 20 CERDIP* | ±2 |

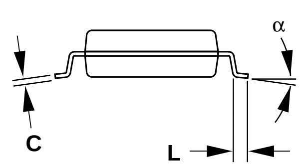
**Contact factory for availability and processing to MIL-STD-883.*

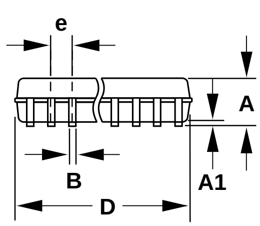
## Chip Information

TRANSISTOR COUNT: 4337

## Package Information




**SSOP SHRINK SMALL-OUTLINE PACKAGE**

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.068 | 0.078 | 1.73 | 1.99 |
| A1 | 0.002 | 0.008 | 0.05 | 0.21 |
| B | 0.010 | 0.015 | 0.25 | 0.38 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | SEE VARIATIONS | | | |
| E | 0.205 | 0.209 | 5.20 | 5.38 |
| e | 0.0256 BSC | | 0.65 BSC | |
| H | 0.301 | 0.311 | 7.65 | 7.90 |
| L | 0.025 | 0.037 | 0.63 | 0.95 |
| α | 0˚ | 8˚ | 0˚ | 8˚ |

| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 14 | 0.239 | 0.249 | 6.07 | 6.33 |
| D | 16 | 0.239 | 0.249 | 6.07 | 6.33 |
| D | 20 | 0.278 | 0.289 | 7.07 | 7.33 |
| D | 24 | 0.317 | 0.328 | 8.07 | 8.33 |
| D | 28 | 0.397 | 0.407 | 10.07 | 10.33 |

21-0056A

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