19-3174; Rev 0; 1/04

EVALUATION KIT AVAILABLE

Low-Cost Linear-Regulator LCD Panel Power Supplies

General Description

The MAX8710/MAX8711/MAX8712 offer complete linear-regulator power-supply solutions for thin-film transistor (TFT) liquid-crystal-display (LCD) panels used in LCD monitors and LCD TVs. All three devices include a high-performance AVDD linear regulator, a positive charge-pump regulator, a negative charge-pump regulator, and built-in power-up sequence control. The MAX8710 and MAX8711 also include a high-current operational amplifier. Additionally, the MAX8710 provides logic-controlled high-voltage switches to control the positive charge-pump output.

The linear regulator directly steps down the input voltage to generate the supply voltage for the source-driver ICs (AVDD). The two built-in charge-pump regulators are used to generate the TFT gate-on and gate-off supplies. The high-current operational amplifier is typically used to drive the LCD backplane (VCOM) and features high output current (150mA), fast slew rate (12V/µs), and wide bandwidth (12MHz). Its Rail-to-Rail® inputs and output maximize flexibility.

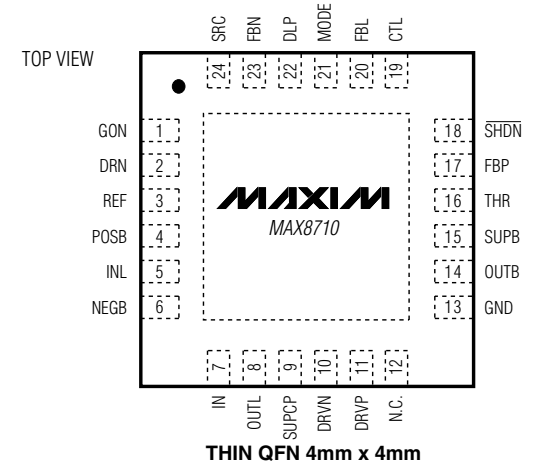
The MAX8710 is available in a 24-pin thin QFN package, the MAX8711 is available in a 16-pin thin QFN package, and the MAX8712 is available in a 12-pin thin QFN package. All three packages are 4mm x 4mm with a maximum thickness of 0.8mm for ultra-thin LCD panel design. They operate over the -40°C to +100°C temperature range.

Applications

LCD Monitor Panel Modules

LCD TV Panel Modules

Pin Configurations



THIN QFN 4mm x 4mm

Pin Configurations continued at end of data sheet.

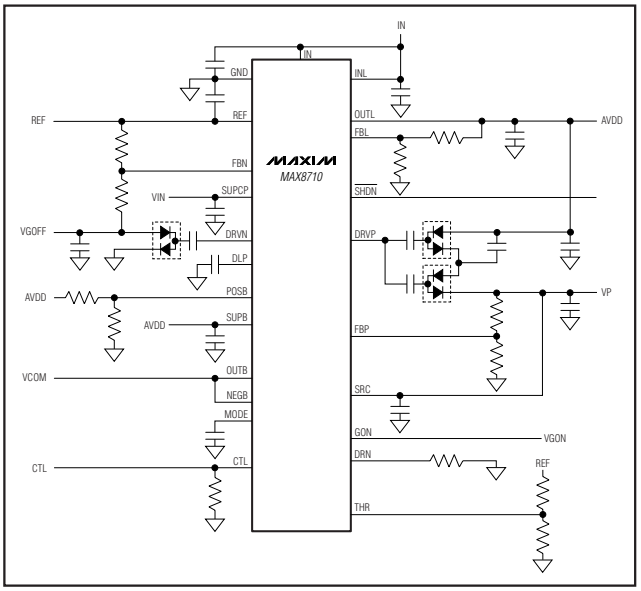
Features

- **High-Performance Linear Regulator**
  - **1.6% Output Accuracy**
  - **Works with Small Ceramic Output Capacitors**
  - **Fast Transient Response**
  - **Foldback Current Limit**
- **50mA Negative Regulated Charge Pump**
- **20mA Positive Regulated Charge Pump with Adjustable Delay**
- **Built-In Power-Up Sequence**
- **High-Current Operational Amplifier (MAX8710/MAX8711)**
  - **±150mA Output Short-Circuit Current**
  - **12V/µs Slew Rate**
  - **12MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs/Output**
- **Dual-Mode™ High-Voltage Switches (MAX8710)**
- **Thermal Protection**
- **Latched Fault Protection with Timer**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8710ETG	-40°C to +100°C	24 Thin QFN 4mm x 4mm
MAX8711ETE	-40°C to +100°C	16 Thin QFN 4mm x 4mm
MAX8712ETC	-40°C to +100°C	12 Thin QFN 4mm x 4mm

Minimum Operating Circuit



Rail-to-Rail is a registered trademark of Motorola, Ltd. Dual Mode is a trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Cost Linear-Regulator LCD Panel Power Supplies

ABSOLUTE MAXIMUM RATINGS

CTL, FBL, FBP, FBN, $\overline{SHDN}$, REF, THR to GND .....-0.3V to +6V
MODE, DLP to GND .....-0.3V to V_{REF} + 0.3V
IN, INL, OUTL (MAX8710) to GND .....-0.3V to +28V
SUPCP, SUPB , OUTL (MAX8711, MAX8712) to GND.....-0.3V to +14V
POSB, OUTB, NEGB to GND .....-0.3V to V_{SUPB} + 0.3V
DRVN, DRVP to GND .....-0.3V to V_{SUPCP} + 0.3V
SRC to GND .....-0.3V to +30V
GON, DRN to GND.....-0.3V to V_{SRC} + 0.3V
DRN to GON.....-30V to +30V
OUTB Maximum Continuous Output Current.....±75mA
DRVP RMS Output Current 90mA
DRVN RMS Output Current.....-150mA
Continuous Power Dissipation (T_A = +70°C) 24-, 16-, and 12-Pin Thin QFN 4mm x 4mm (derate 16.9mW/°C above +70°C).....1349mW
Operating Temperature Range .....-40°C to +100°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 27V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Operating Supply Range		8		28	V
IN Quiescent Current	$\overline{SHDN}$ = GND		0.2	0.4	mA
	$\overline{SHDN}$ = 3.3V			2.5	
Duration to Trigger Fault Condition	2^{16} oscillator clock cycles		44		ms
REF Output Voltage	-10µA < I_{REF} < 1mA (excluding internal load)	4.9	5.0	5.1	V
SUPCP Input Supply Range		2.7		13.2	V
Charge-Pump Regulators Operating Frequency		1275	1500	1725	kHz
Thermal Shutdown	Rising temperature, 15°C hysteresis		+160		°C
LINEAR REGULATOR					
INL Operation Supply Range	V_{OUTL} < V_{INL}	7		28	V
Dropout Voltage	I_{OUTL} = 50mA		150	300	mV
FBL Regulation Voltage	I_{OUTL} = 50mA	2.46	2.50	2.54	V
FBL Input Bias Current	V_{FBL} = 2.5V			50	nA
FBL Fault Trip Level	Falling edge	1.92	2.00	2.08	V
FBL Line-Regulation Error	V_{INL} = V_{IN} = 10.8V~13.2V, V_{OUTL} = 10V, I_{OUTL} = 50mA			15	mV
	V_{INL} = V_{IN} = 10V~28V, V_{OUTL} = 9V, I_{OUTL} = 50mA		10		
Bandwidth	Guaranteed by design	1000			kHz
Maximum OUTL Current	V_{FBL} = 2.4V	300			mA
OUTL Soft-Start Period	2^{12} oscillator clock cycles in a 7-bit DAC		3		ms
OUTL Load Regulation	V_{IN} = 12V, 5mA < I_{OUTL} < 300mA			2	%
OPERATIONAL AMPLIFIER					
SUPB Supply Operating Range		4.5		13.2	V
SUPB Supply Current	Buffer configuration, V_{POSB} = 4V, no load		0.7	1.0	mA
Input Offset Voltage	(V_{NEGB}, V_{POSB}) = V_{SUPB} / 2, T_A = +25°C		0	12	mV
Input Bias Current	(V_{NEGB}, V_{POSB}) = V_{SUPB} / 2	-50	+1	+50	nA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 27V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Input Range	V_{NEGB}, V_{POSB}	0		V_{SUPB}	V
Common-Mode Rejection Ratio	0 ≤ (V_{NEGB}, V_{POSB}) < V_{SUPB}	50	90		dB
Open-Loop Gain			125		dB
Output Voltage Swing High	I_{OUTB} = 100µA	V_{SUPB} - 15	V_{SUPB} - 2		mV
	I_{OUTB} = 5mA	V_{SUPB} - 150	V_{SUPB} - 80		
Output Voltage Swing Low	I_{OUTB} = -100µA		2	15	mV
	I_{OUTB} = -5mA		80	150	
Short-Circuit Current	Short to V_{SUPB} / 2, sourcing	50	150		mA
	Short to V_{SUPB} / 2, sinking	50	140		
Output Current	Buffer configuration, V_{POSB} = 4V, V_{OUTB} error < ±10mV		±40		mA
Power-Supply Rejection Ratio	6V ≤ V_{SUPB} ≤ 13.2V, DC (V_{NEGB}, V_{POSB}) = V_{SUPB} / 2	60	100		dB
Slew Rate			12		V/µs
-3dB Bandwidth	Buffer configuration, R_L = 10kΩ, C_L = 10pF		12		MHz
Gain-Bandwidth Product	Buffer configuration, R_L = 10kΩ, C_L = 10pF		8		MHz
POSITIVE CHARGE-PUMP REGULATOR					
FBP Regulation Voltage	I_{GON} = 10mA	2.425	2.500	2.575	V
FBP Line-Regulation Error	V_{OUTL} (V_{SUPCP}, MAX8710) = 10.8V~13.2V, V_{GON} = 27V, I_{GON} = 20mA			25	mV
FBP Input Bias Current	V_{FBP} = 2.5V	-50		+50	nA
DRVP P-Channel On-Resistance			15	30	Ω
DRVP N-Channel On-Resistance	V_{FBP} = 2.4V		6	12	Ω
	V_{FBP} = 2.6V	20			kΩ
FBP Fault Trip Level	Falling edge	1.92	2.00	2.08	V
Positive Charge-Pump Soft-Start Period	2^{12} oscillator clock cycles in a 7-bit DAC		2.73		ms
NEGATIVE CHARGE-PUMP REGULATOR					
FBN Regulation Voltage	I_{GOFF} = 10mA	200	250	300	mV
FBN Input Bias Current	V_{FBN} = 250mV	-50		+50	nA
FBN Line Regulation	V_{OUTL} (V_{SUPCP}, MAX8710) = 10.8V~13.2V, V_{VGOFF} = -6V, I_{GOFF} = -50mA			25	mV
DRVN P-Channel On-Resistance			7.5	15	Ω
DRVN N-Channel On-Resistance	V_{FBN} = 350mV		3	6	Ω
	V_{FBN} = 150mV	20			kΩ
FBN Fault Trip Level	Rising edge		700		mV
Negative Charge-Pump Soft-Start Period	2^{12} oscillator clock cycles in a 7-bit DAC		2.73		ms

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 27V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SEQUENCE CONTROL					
$\overline{SHDN}$ Input Low Voltage				0.6	V
$\overline{SHDN}$ Input High Voltage		2.0			V
$\overline{SHDN}$ Input Current				1	µA
DLP Capacitor Charge Current	During startup, V_{DLP} = 1.0V	4	5	6	µA
DLP Turn-On Threshold		2.375	2.5	2.625	V
Pin Discharge Switch On-Resistance	$\overline{SHDN}$ = low or fault tripped; DLP, FBP, FBN to GND		10		Ω
	$\overline{SHDN}$ = low or fault tripped; MODE, OUTL, GON, OUTB to GND		1		kΩ
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		2.0			V
CTL Input Leakage Current		-1		+1	µA
CTL to GON Rising Propagation Delay	V_{MODE} = V_{REF}, 1.5nF from GON to GND, V_{CTL} = 0V to 3V step, no load on GON, measured from V_{CTL} = 1.5V to GON = 20%		100		ns
CTL to GON Falling Propagation Delay	V_{MODE} = V_{REF}, 1.5nF from GON to GND, V_{CTL} = 3V to 0V step, DRN falling, no load on DRN and GON, measured from V_{CTL} = 1.5V to GON = 80%		100		ns
SRC Input Voltage Range				28	V
SRC Input Current	V_{MODE} = V_{REF}, VDLP = 3V, CTL = high		150	250	µA
DRN Input Current	V_{MODE} = V_{REF}, VDRN = 8V, VDLP = 3V, VCTL = 0V		26	40	µA
SRC Switch On-Resistance	V_{MODE} = V_{REF}, VDLP = 3V, CTL = high		15	30	Ω
DRN Switch On-Resistance	V_{MODE} = V_{REF}, VDLP = 3V, VCTL = 0V		30		Ω
MODE Switch On-Resistance			1		kΩ
Mode 2 MODE Capacitor Charge Current	V_{MODE} < MODE current-source stop voltage threshold	42	50	64	µA
MODE Voltage Threshold for Enabling DRN Switch Control in Mode 2		2.3	2.5	2.7	V
MODE Current-Source Stop Voltage Threshold	V_{MODE} rising edge	3.3	3.5	3.7	V
THR to GON Voltage Gain		9.4	10	10.6	V/V
GON Falling Slew Rate			13.5		V/µs

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 27V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REF Output Voltage	-10µA < I_{REF} < 1mA (excluding internal load)	4.9		5.1	V
SUPCP Input Supply Range		2.7		13.2	V
Charge-Pump Regulators Operating Frequency		1200		1850	kHz
LINEAR REGULATOR					
Dropout Voltage	I_{OUTL} = 50mA			300	mV
FBL Regulation Voltage	I_{OUTL} = 50mA	2.455		2.545	V
FBL Fault Trip Level	Falling edge	1.96		2.04	V
FBL Line-Regulation Error	V_{INL} = V_{IN} = 10.8V~13.2V, V_{OUTL} = 10V, I_{OUTL} = 50mA			15	mV
Maximum OUTL Current	V_{FBL} = 2.4V	300			mA
OUTL Load Regulation	V_{IN} = 12V, 5mA < I_{OUTL} < 300mA			2	%
OPERATIONAL AMPLIFIER					
SUPB Supply Current	Buffer configuration, V_{POSB} = 4V, no load			1.0	mA
Input Offset Voltage	(V_{NEGB}, V_{POSB}) = V_{SUPB} / 2			14	mV
Output Voltage Swing High	I_{OUTB} = 100µA	V_{SUPB} - 15			mV
	I_{OUTB} = 5mA	V_{SUPB} - 150			
Output Voltage Swing Low	I_{OUTB} = -100µA			15	mV
	I_{OUTB} = -5mA			150	
Short-Circuit Current	Short to V_{SUPB} / 2, sourcing	50			mA
	Short to V_{SUPB} / 2, sinking	50			
POSITIVE CHARGE-PUMP REGULATOR					
FBP Regulation Voltage	I_{GON} = 10mA	2.425		2.575	V
FBP Line-Regulation Error	V_{OUTL} (V_{SUPCP}, MAX8710) = 10.8V~13.2V, V_{GON} = 27V, I_{GON} = 20mA			25	mV
FBP Input Bias Current	V_{FBP} = 3V	-50		+50	nA
DRVP P-Channel On-Resistance				30	Ω
DRVP N-Channel On-Resistance	V_{FBP} = 2.4V			12	Ω
	V_{FBP} = 2.6V	20			kΩ
NEGATIVE CHARGE-PUMP REGULATOR					
FBN Regulation Voltage	I_{GOFF} = 10mA	200		300	mV
FBN Line Regulation	V_{OUTL} (V_{SUPCP}, MAX8710) = 10.8V~13.2V, V_{GOFF} = -6V, I_{GOFF} = -50mA			25	mV
DRVN P-Channel On-Resistance				15	Ω
DRVN N-Channel On-Resistance	V_{FBN} = 350mV			6	Ω
	V_{FBN} = 150mV	20			kΩ

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 27V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 1)

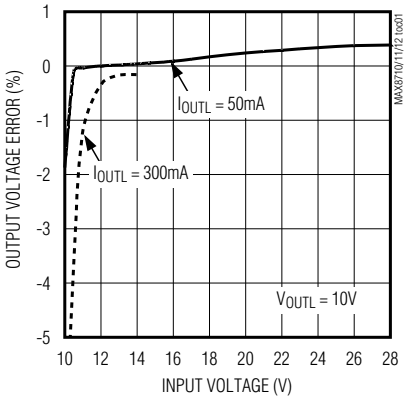
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SEQUENCE CONTROL					
$\overline{SHDN}$ Input Low Voltage				0.6	V
$\overline{SHDN}$ Input High Voltage		2.0			V
DLP Capacitor Charge Current	During startup, V_{DLP} = 1.0V	4		6	µA
DLP Turn-On Threshold		2.375		2.625	V
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
SRC Input Current	V_{MODE} = V_{REF}, V_{DLP} = 3V, CTL = high			250	µA
DRN Input Current	V_{MODE} = V_{REF}, V_{DRN} = 8V, V_{DLP} = 3V, V_{CTL} = 0V			40	µA
SRC Switch On-Resistance	V_{MODE}=V_{REF}, V_{DLP} = 3V, CTL = high			30	Ω
Mode 2 MODE Capacitor Charge Current	V_{MODE} < MODE current-source stop voltage threshold	42		64	µA
MODE Voltage Threshold for Enabling DRN Switch Control in Mode 2		2.3		2.7	V

Note 1: Specifications to -40°C and +100°C are guaranteed by design, not production tested.

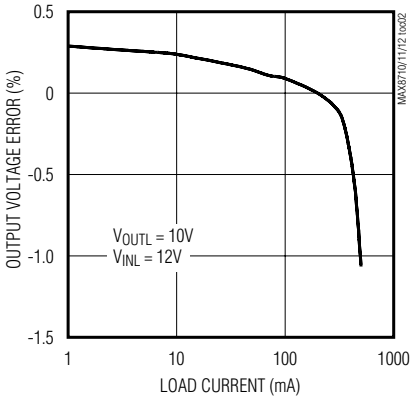
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 10V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.)

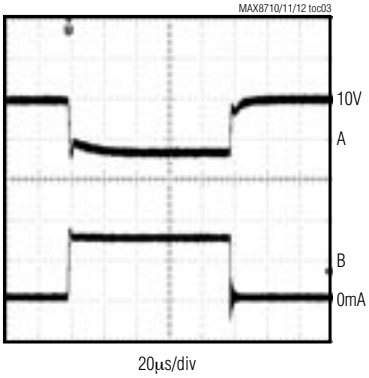
LINEAR-REGULATOR LINE REGULATION



LINEAR-REGULATOR LOAD REGULATION



LINEAR-REGULATOR LOAD-TRANSIENT RESPONSE

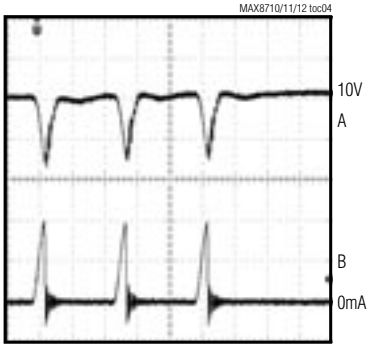


A: V_{OUTL}, 50mV/div, AC-COUPLED
B: I_{OUTL}, 200mA/div

Typical Operating Characteristics (continued)

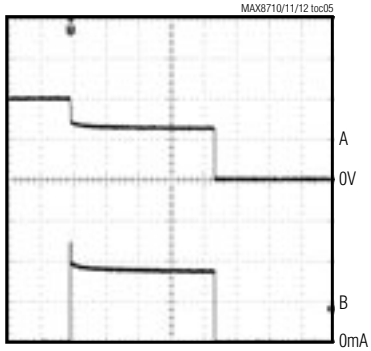
(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 10V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.)

LINEAR-REGULATOR PULSED LOAD-TRANSIENT RESPONSE



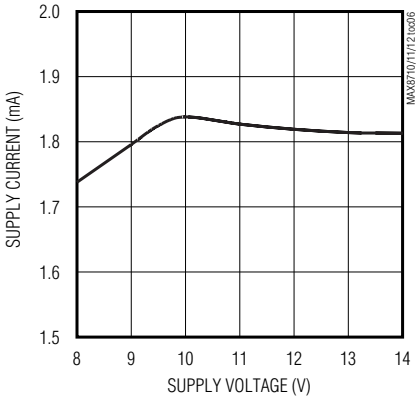
A: V_{OUTL}, 100mV/div, AC-COUPLED
B: I_{OUTL}, 500mA/div

LINEAR-REGULATOR OVERCURRENT PROTECTION

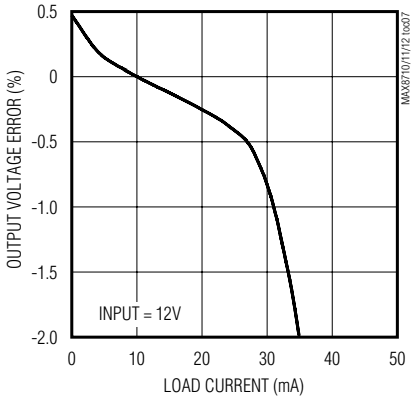


A: V_{OUTL}, 5V/div
B: I_{OUTL}, 500mA/div

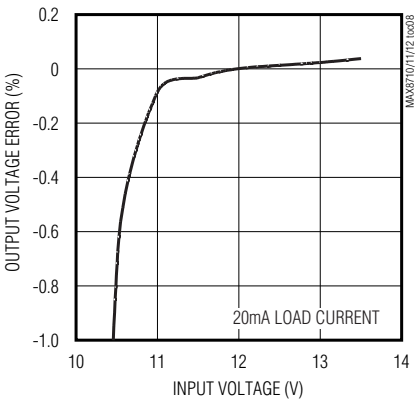
CHARGE-PUMP NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



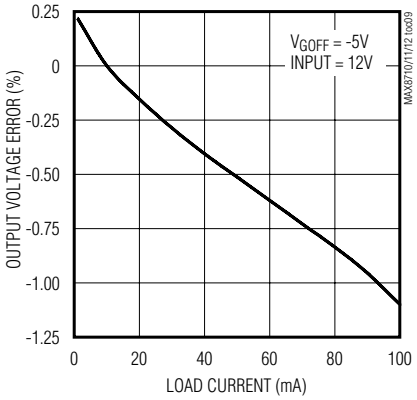
POSITIVE CHARGE-PUMP LOAD REGULATION



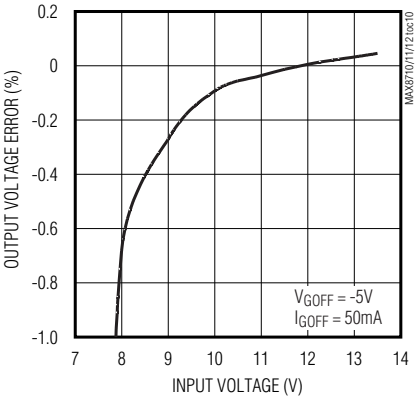
POSITIVE CHARGE-PUMP LINE REGULATION



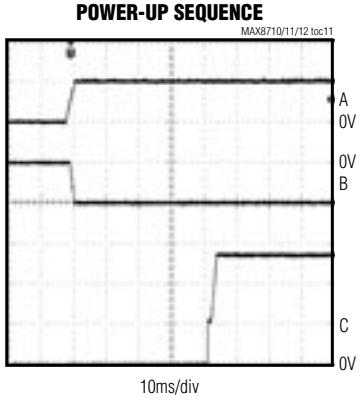
NEGATIVE CHARGE-PUMP LOAD REGULATION



NEGATIVE CHARGE-PUMP LINE REGULATION

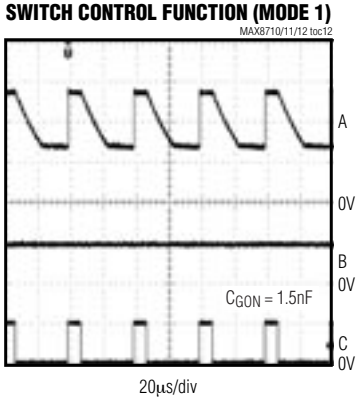


POWER-UP SEQUENCE



A: V_{OUTL}, 10V/div
B: V_{GOFF}, 5V/div
C: V_{GON}, 10V/div

SWITCH CONTROL FUNCTION (MODE 1)



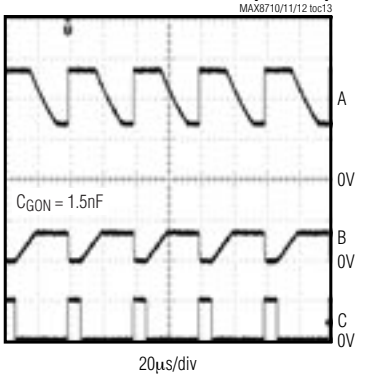
A: V_{GON}, 10V/div
B: V_{MODE}, 5V/div
C: V_{CTL}, 5V/div

Low-Cost Linear-Regulator LCD Panel Power Supplies

Typical Operating Characteristics (continued)

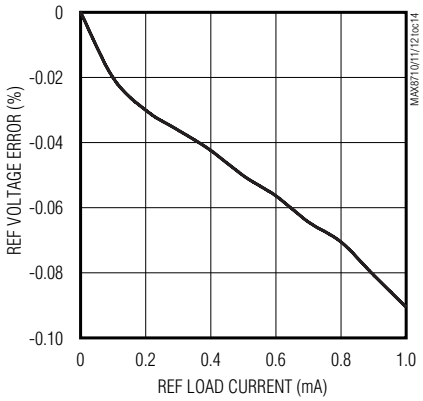
(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPCP} = 12V, V_{OUTL} = V_{SUPB} = 10V, V_{SRC} = 10V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.)

SWITCH CONTROL FUNCTION (MODE 2)

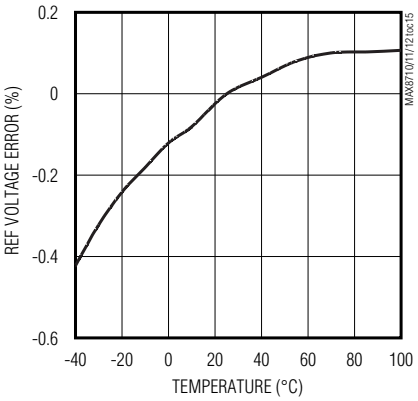


A: V_{GON}, 10V/div
B: V_{MODE}, 5V/div
C: V_{CTL}, 5V/div

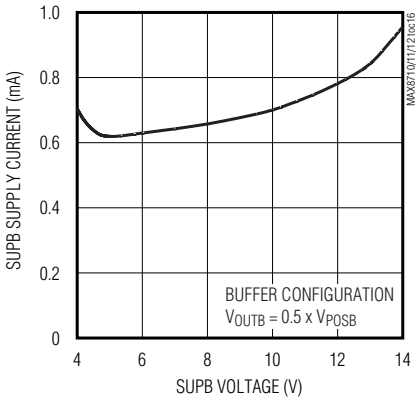
REFERENCE LOAD REGULATION



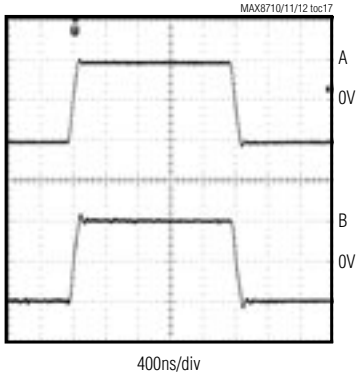
REFERENCE vs. TEMPERATURE



SUPB SUPPLY CURRENT vs. SUPB VOLTAGE

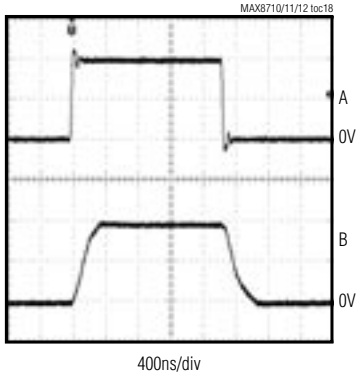


OPERATIONAL-AMPLIFIER SMALL-SIGNAL STEP RESPONSE (BUFFER CONFIGURATION)



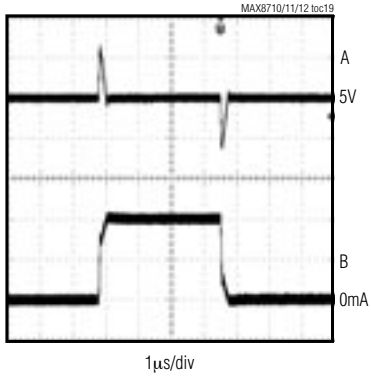
A: V_{POSB}, 50mV/div, AC-COUPLED
B: V_{OUTB}, 50mV/div, AC-COUPLED

OPERATIONAL-AMPLIFIER LARGE-SIGNAL STEP RESPONSE (BUFFER CONFIGURATION)



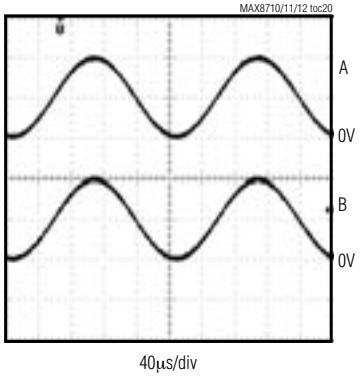
A: V_{POSB}, 5V/div
B: V_{OUTB}, 5V/div

OPERATIONAL-AMPLIFIER LOAD-TRANSIENT RESPONSE (BUFFER CONFIGURATION)



A: V_{OUTB}, 2V/div
B: I_{OUTB}, 50mA/div

OPERATIONAL-AMPLIFIER RAIL-TO-RAIL I/O



A: V_{POSB}, 5V/div
B: V_{OUTB}, 5V/div

Pin Description

NAME	PIN			FUNCTION
	MAX8710	MAX8711	MAX8712	
GON	1	—	—	Internal High-Voltage MOSFET Switch Common Terminal. GON is the output of the high-voltage switch-control block. GON is internally pulled to GND by a 1kΩ resistor in shutdown.
DRN	2	—	—	Switch Input. Drain of the internal high-voltage back-to-back P-channel MOSFETs connected to GON.
REF	3	1	1	Reference Output. Connect a 0.22µF capacitor from REF to GND. REF remains on in shutdown.
POSB	4	2	—	Operational-Amplifier Noninverting Input
INL	5	3	2	Linear-Regulator Supply Input
NEGB	6	4	—	Operational-Amplifier Inverting Input
IN	7	5	3	IC Supply Input. Bypass IN to GND with a 0.1µF capacitor.
OUTL	8	6	4	Linear-Regulator Output. OUTL is internally pulled to GND by a 1kΩ resistor in shutdown. For the MAX8711/MAX8712, OUTL is also the supply input for the charge-pump regulators.
SUPCP	9	—	—	Supply Input for the Charge-Pump Regulators. Connect a 0.1µF capacitor from SUPCP to GND.
DRVN	10	7	5	Negative Charge-Pump Driver Output. Output high level is V_{SUPCP}, and output low level is GND. DRVN is internally pulled high to SUPCP when the negative charge pump is disabled.
DRVP	11	8	6	Positive Charge-Pump Driver Output. Output high level is V_{SUPCP}, and output low level is GND. DRVP is internally pulled low in shutdown.
N. C.	12	—	—	No Connect. Not internally connected.
GND	13	9	7	Ground
OUTB	14	10	—	Operational-Amplifier Output. OUTB is internally pulled to GND by a 1kΩ resistor in shutdown.
SUPB	15	11	—	Operational-Amplifier Supply Input. Bypass SUPB to GND with a 0.1µF capacitor.
THR	16	—	—	GON Low-Level Regulation Set-Point Input. Connect THR to the center of a resistive voltage-divider between REF and GND to set the V_{GON} regulation level. The actual level is $10 \times V_{THR}$. See the *Switch Control* section for details.

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Pin Description (continued)

NAME	PIN			FUNCTION
	MAX8710	MAX8711	MAX8712	
FBP	17	12	8	Positive Charge-Pump Feedback Input. Connect FBP to the center of a resistive voltage-divider between the positive charge-pump regulator output and GND to set the regulator output voltage. Place the divider within 5mm of FBP. FBP is internally pulled to GND by a 10Ω resistor in shutdown.
$\overline{SHDN}$	18	13	9	Active-Low Shutdown Control Input. Pull $\overline{SHDN}$ low to turn off all sections of the device except REF. Pull $\overline{SHDN}$ high to enable the device. Cycle $\overline{SHDN}$ to reset the device after a fault.
CTL	19	—	—	High-Voltage Switch-Control Block Timing Control Input. See the *Switch Control* section for details.
FBL	20	14	10	Linear-Regulator Feedback Input. Connect FBL to the center of a resistive voltage-divider between the linear-regulator output and GND to set the linear-regulator output voltage. Place the divider within 5mm of FBL.
MODE	21	—	—	High-Voltage Switch-Control Block-Mode Selection Input and Timing-Adjustment Input. See the *Switch Control* section for details. MODE is high impedance when it is connected to REF. MODE is internally pulled to GND by a 1kΩ resistor during REF UVLO, when V_{DLP} < 2.5V, or in shutdown.
DLP	22	15	11	Positive Charge-Pump Startup Delay and High-Voltage Switch Delay Input. Connect a capacitor from DLP to GND to set the delay time. A 5µA current source charges C_{DLP}. DLP is internally pulled to GND by a 10Ω resistor in shutdown.
FBN	23	16	12	Negative Charge-Pump Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and REF to set the output voltage. Place the divider within 5mm of FBN. FBN is internally pulled to GND through a 10Ω resistor in shutdown.
SRC	24	—	—	Switch Input. Source of the internal high-voltage P-channel MOSFET connected to GON.

Typical Operating Circuit

Figures 1, 2, and 3 are the *Typical Operating Circuits* of the MAX8710, MAX8711, and MAX8712 for generating power rails in TFT LCD panels. The input voltage range is from 10.8V to 13.2V. The AVDD output is 10V at 300mA, the V_{GON} output is 27V at 20mA, and the V_{GOFF} output is -5V at 50mA.

Detailed Description

The MAX8710/MAX8711/MAX8712 include a high-performance linear regulator, a positive charge-pump regulator, a negative charge-pump regulator, and built-in power-up sequence control. The MAX8710 and MAX8711 also include a high-current operational amplifier. Additionally, the MAX8710 provides logic-controlled high-voltage switches to control the positive charge-pump output. The linear regulator directly steps down the input voltage to generate the source-driver ICs' supply voltage. The two built-in charge-pump regulators are used to generate the TFT gate-on and gate-off supplies. The high-current operational amplifier is typically used to drive the LCD backplane (VCOM) and features high output current (150mA), fast slew rate (12V/µs), and wide bandwidth (12MHz). Its rail-to-rail inputs and output maximize flexibility.

Linear Regulator

MAX8710/MAX8711/MAX8712 contain a linear regulator that uses an internal PNP pass transistor to supply load currents up to 300mA. Connect an external resistive voltage-divider between the regulator output and GND with the midpoint connected to FBL to adjust the linear-regulator output. An error amplifier compares the FBL voltage with the 2.5V internal reference voltage and amplifies the difference. If the feedback voltage is higher than the

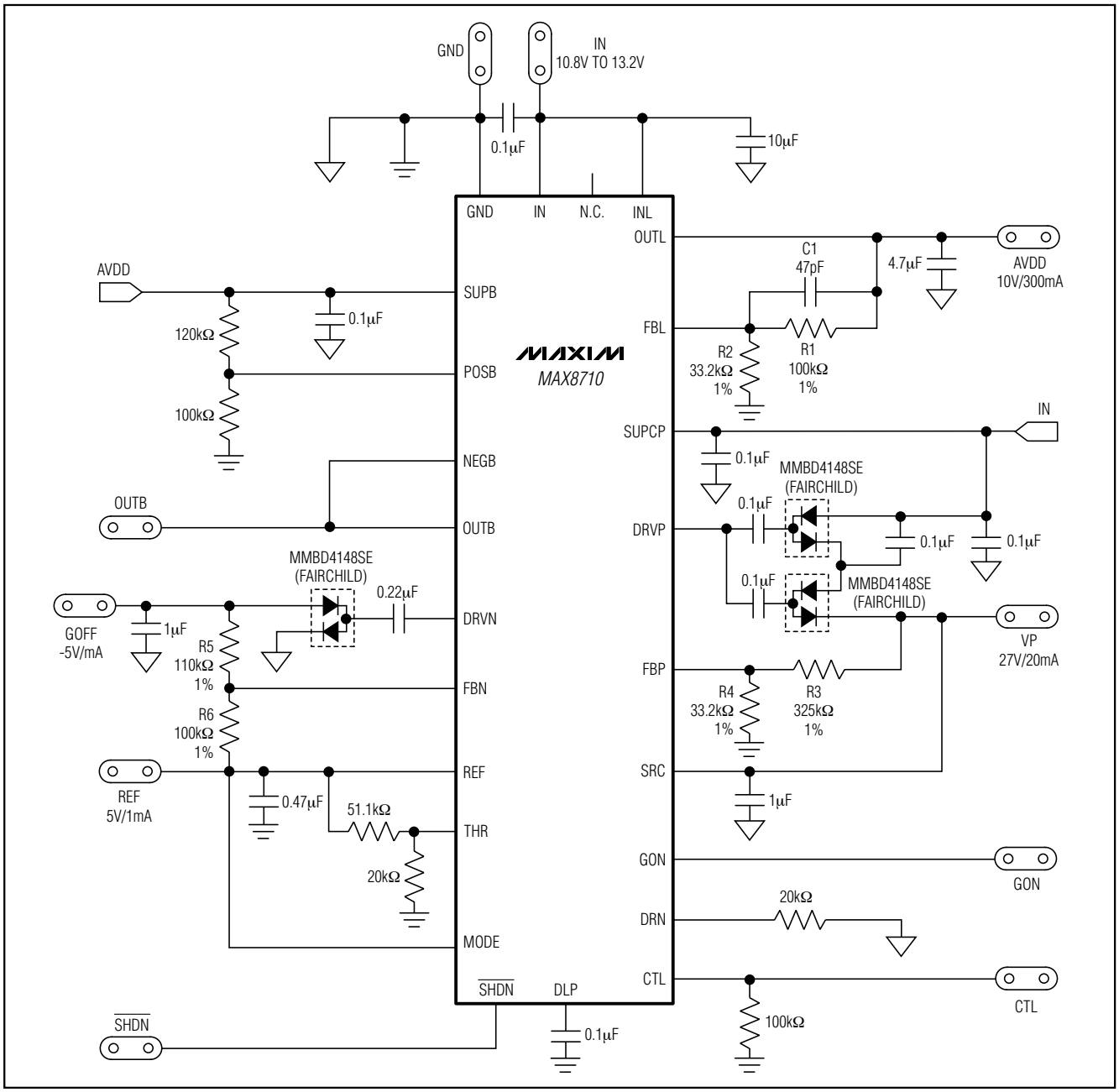

Figure 1. Typical Operating Circuit of the MAX8710

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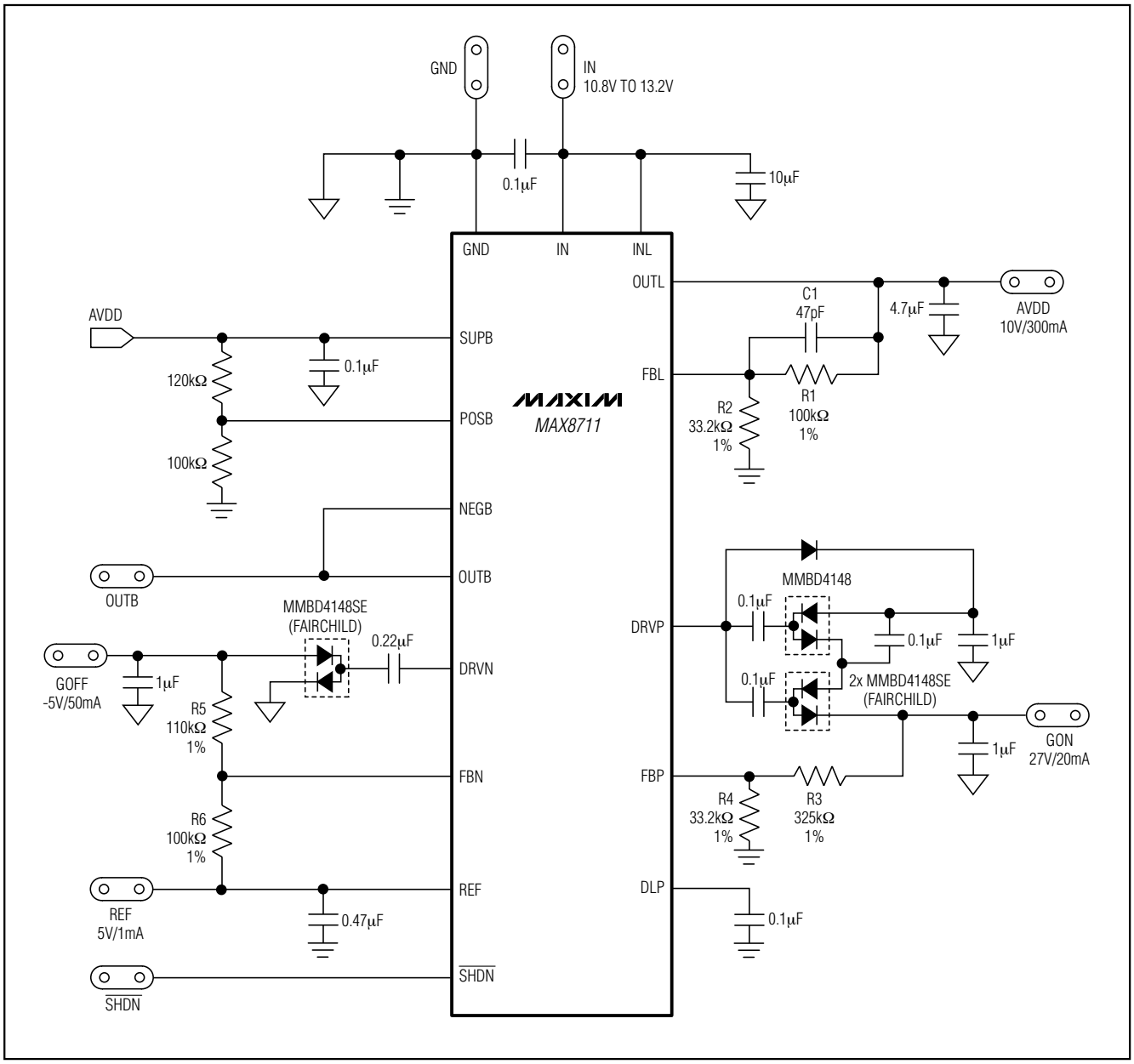

Figure 2. Typical Operating Circuit of the MAX8711

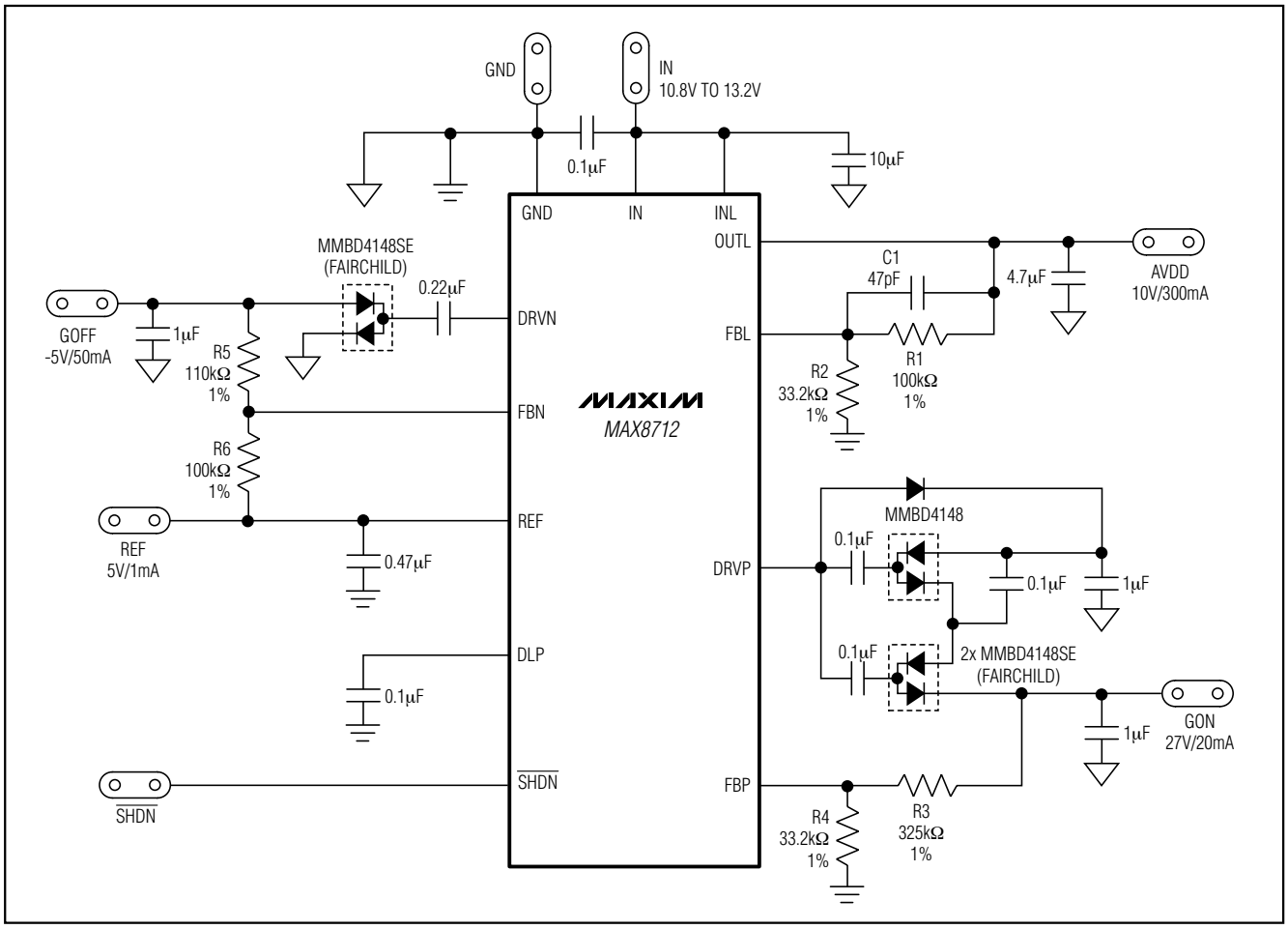

Figure 3. Typical Operating Circuit of the MAX8712

reference voltage, the controller lowers the base current of the PNP transistor, which reduces the amount of current delivered to the output. If the feedback voltage is too low, the device increases the PNP transistor's base current, which allows more current to pass to the output and raises the output voltage. The linear regulator also includes an output current limit that protects the internal pass transistor against short circuits.

The input voltage range of the linear regulator is from 8V to 28V. The *Typical Operating Circuits* shown use a 12V input. The output voltage range of the linear regulator (OUTL) is up to 28V (MAX8710) or up to 14V (MAX8711/MAX8712). The linear-regulator output is used to generate the AVDD voltage, which is the analog supply rail for source-driver ICs in TFT LCD panels. The typical load of the AVDD supply is a periodic pulsed load, with a peak current of approximately 1A and pulse width of approximately 2µs. The period of the pulse load is between 8.9µs and 31.7µs. The excellent transient performance of the linear regulator can easily meet this transient-response requirement.

The linear regulator can deliver at least 300mA output current continuously with a 4.7µF output capacitor. Do not allow the device power dissipation to exceed the package-dissipation limit listed in the *Absolute Maximum Ratings* section. The power dissipation can be estimated by multiplying the voltage difference between the input and the output with the required maximum continuous output current. For applications where the power dissipation exceeds the package limit, see the *External Transistor for Higher Current or Power Dissipation* section for more information.

The linear regulator is enabled whenever REF is in regulation and $\overline{SHDN}$ is logic high. Each time it is enabled, the

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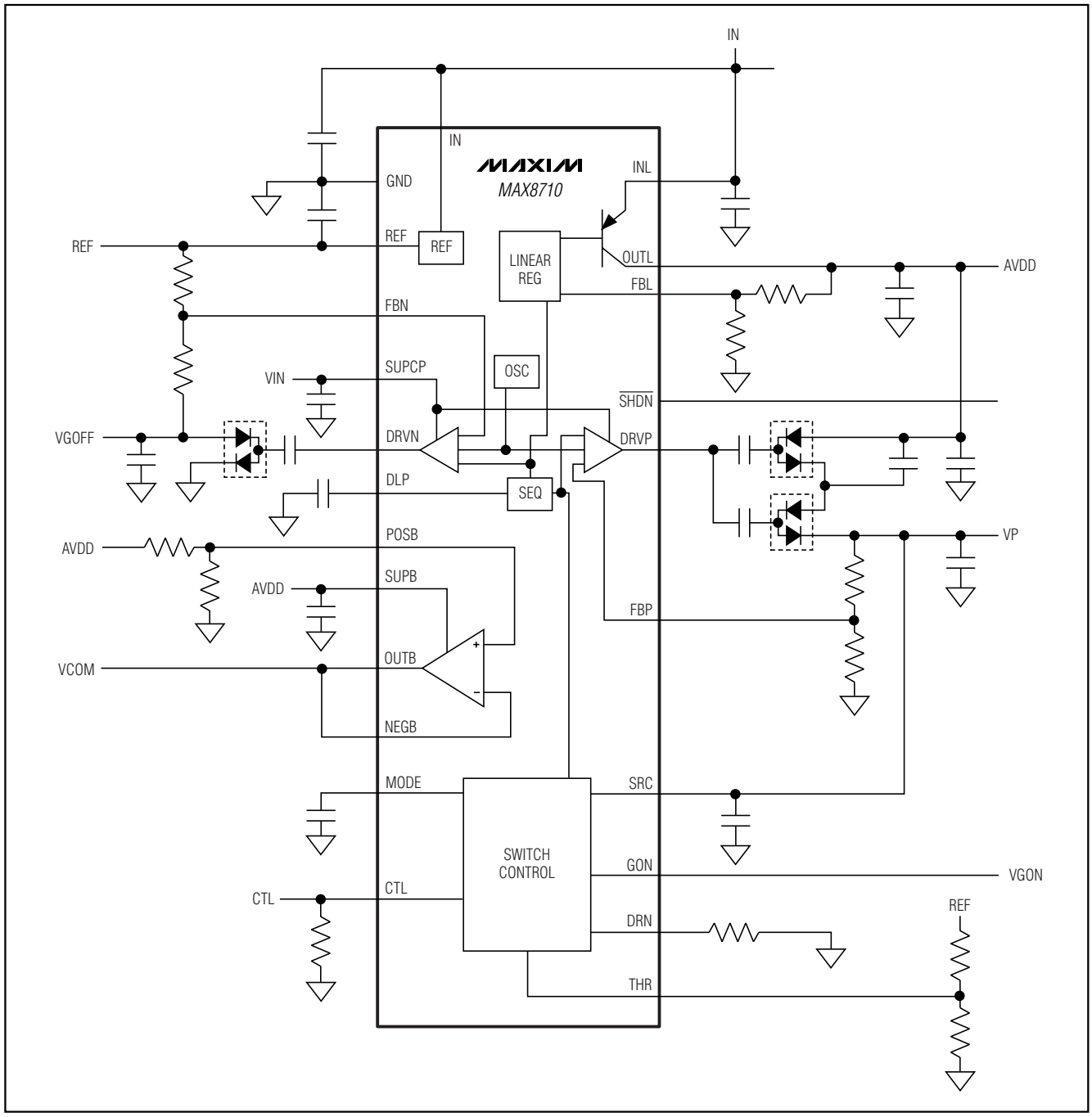

Figure 4. MAX8710 Functional Diagram

linear regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 2.5V in 128 steps. The soft-start period is 2.73ms (typ), and FBL fault detection is disabled during this period. This soft-start feature effectively limits the inrush current during startup.

The linear-regulator current-limit circuitry monitors the current flowing through the internal pass transistor. The internal current limit is approximately 800mA. The linear-regulator output declines when it is not able to supply the load current. If the FBL voltage drops below 0.75V, the current limit folds back to approximately 100mA.

The MAX8710/MAX8711/MAX8712 monitor the FBL voltage for undervoltage conditions. If V_{FBL} is continuously below 2V (typ) for approximately 44ms, the device latches off. The foldback current-limit circuit, in conjunction with the output undervoltage fault latch and thermal-overload protection, protects the output load and the internal pass transistor against short circuits or overloads.

Positive Charge-Pump Regulator

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate-driver ICs. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The number of charge-pump stages and the setting of the feedback divider determine the output voltage of the positive charge-pump regulator. The charge pump includes a high-side P-channel MOSFET (P1) and a low-side N-channel MOSFET (N1) to control the power transfer as shown in Figure 5. The MOSFETs switch at a constant frequency of 1.5MHz.

During the first half-cycle, N1 turns on and allows V_{INPUT} (V_{SUPCP}, MAX8710 or VOUTL, MAX8711/MAX8712) to charge up the flying capacitor $C_{X(POS)}$ through diode D1. The amount of charge transferred from V_{INPUT} to $C_{X(POS)}$ is determined by the on-resistance of N1, which varies according to the output of the feedback error amplifier. The error amplifier compares the feedback signal (FBP) with a 2.5V internal reference and amplifies the difference. If the feedback signal is below the reference, the error-amplifier output increases the supply voltage of N1's gate driver, lowering the on-resistance. Similarly, if the feedback signal is above the reference, the error-amplifier output reduces the driver supply voltage, increasing the on-resistance. During the second half-cycle, N1 turns off and P1 turns on, level shifting $C_{X(POS)}$ by V_{INPUT} volts. This connects $C_{X(POS)}$ in parallel with the reservoir capacitor $C_{OUT(POS)}$. If the voltage across $C_{OUT(POS)}$ plus a diode drop (V_{POS} + V_{DIODE}) is smaller than the level-shifted flying-capacitor voltage

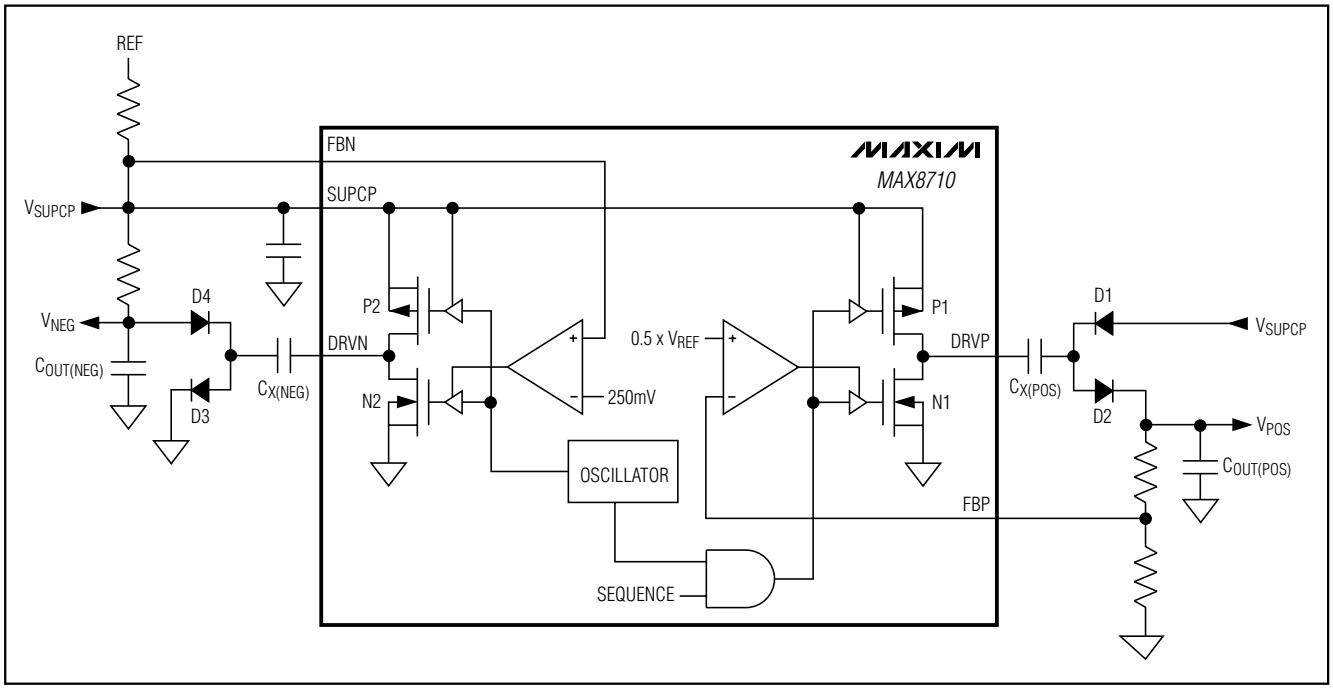

Figure 5. Charge-Pump Regulator Functional Diagram

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($V_{CX(POS)}$ + V_{INPUT}), charge flows from $C_{X(POS)}$ to $C_{OUT(POS)}$ until diode D2 turns off.

The positive charge-pump regulator's startup can be delayed by connecting an external capacitor from DLP to GND. An internal constant current source begins charging the DLP capacitor when $\overline{SHDN}$ is logic high and REF reaches regulation. When the DLP voltage exceeds V_{REF} / 2, the positive charge-pump regulator is enabled. Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 2.5V in 128 steps. The soft-start period is 2.73ms (typ), and FBP fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup. The MAX8710/MAX8711/MAX8712 also monitor the FBP voltage for undervoltage conditions. If V_{FBP} is continuously below 2V (typ) for approximately 44ms, the device latches off.

Negative Charge-Pump Regulator

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate-driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side P-channel MOSFET (P2) and a low-side N-channel MOSFET (N2) to control the power transfer as shown in Figure 5. The MOSFETs switch a constant frequency of 1.5MHz.

During the first half-cycle, P2 turns on and allows V_{INPUT} to charge up the flying capacitor $C_{X(NEG)}$ through diode D3. During the second half-cycle, P2 turns off and N2 turns on, level shifting $C_{X(NEG)}$ by V_{INPUT} volts. This connects $C_{X(NEG)}$ in parallel with reservoir capacitor $C_{OUT(NEG)}$. If the voltage across $C_{OUT(NEG)}$ minus a diode drop is greater than the voltage across $C_{X(NEG)}$, charge flows from $C_{OUT(NEG)}$ to $C_{X(NEG)}$ until the diode D4 turns off. The amount of charge transferred to the output is controlled by the on-resistance of N2, which varies according to the output of the feedback error amplifier. The error amplifier compares the feedback signal (FBN) with a 250mV internal reference and amplifies the difference. If the feedback signal is above the reference, the error-amplifier output increases the supply voltage of N2's gate driver, lowering the on-resistance. Similarly, if the feedback signal is below the reference, the error-amplifier output reduces the driver supply voltage, increasing the on-resistance.

The negative charge-pump regulator is enabled when $\overline{SHDN}$ is logic high and REF reaches regulation. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 5V to 250mV in 128 steps. The soft-start period is 2.73ms (typ), and FBN fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup. The MAX8710/MAX8711/MAX8712 also monitor the FBN voltage for undervoltage conditions. If V_{FBN} is continuously above 700mV (typ) for approximately 44ms, the device latches off.

Operational Amplifier (MAX8710/MAX8711)

The MAX8710/MAX8711s' operational amplifier features high output current (150mA), fast slew rate (7.5V/µs), and wide bandwidth (12MHz). The operational amplifier is enabled when REF is in regulation and $\overline{SHDN}$ is logic high. The output of the amplifier (OUTB) is internally pulled to ground through a 1kΩ resistor in shutdown.

The amplifier is typically used to drive the backplane (VCOM) of TFT LCD panels. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by this operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and its gain peaking increases. To ensure stable operation, a 5Ω to 50Ω resistor can be placed between OUTB and the capacitive load to reduce gain peaking.

The operational amplifier limits short-circuit current to approximately ±150mA if the output is directly shorted to SUPB or to GND. If the short-circuit condition persists, the junction temperature of the IC rises until it trips the IC's thermal-overload protection.

Reference Voltage (REF)

The reference output is nominally 5V and can source up to 1mA (see the *Typical Operating Characteristics*). Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND. The reference remains enabled in shutdown.

Power-Up Sequence and Shutdown Control

When the MAX8710/MAX8711/MAX8712 are powered up, REF rises with the voltage on IN. After REF reaches regulation and if $\overline{SHDN}$ is logic high, the linear regulator, operational amplifier, and negative charge-pump regulator are enabled and begin their respective soft-start routines. After the soft-start routines are complet-

ed, the fault-protection circuits for the linear regulator and the negative charge-pump regulator are activated.

When the linear regulator is enabled, the positive charge-pump-regulator delay block is enabled. An internal current source starts charging the DLP capacitor. The voltage on DLP linearly rises because of the constant charging current. When V_{DLP} goes above V_{REF} / 2, the switch control block is enabled, and the positive charge-pump regulator begins its soft-start. After the positive charge-pump regulator's soft-start is completed, the fault protection of the positive charge-pump regulator is also enabled.

The MAX8710/MAX8711/MAX8712 enter into shutdown when $\overline{SHDN}$ is pulled low or REF falls below 4.5V. In shutdown, OUTL, GON and OUTB are all internally pulled to ground with 1kΩ resistors. FBN, FBP, and DLP are all internally pulled to ground with 10Ω resistors in shutdown. The DLP current source is disabled in shutdown and a switch discharges C_{DLP} to ground. REF remains on in shutdown. Pulling $\overline{SHDN}$ high when REF is above 4.5V reactivates the IC. Output fault protection and thermal-overload protection can also turn off the IC's outputs. See the respective sections for details.

Output Fault Protection

During steady-state operation, if the output of the linear regulator or any of the charge-pump regulator outputs does not exceed its respective fault-detection threshold, the MAX8710/MAX8711/MAX8712 activate an internal fault timer. If any condition or the combination of conditions indicates a continuous fault for the fault-timer duration (44ms typ), the MAX8710/MAX8711/MAX8712 set the fault latch, shutting down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage or toggle $\overline{SHDN}$ to clear the fault latch and reactivate the device. Each regulator's fault-detection circuit is disabled during the regulator's soft-start time.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the IC. When the junction temperature exceeds +160°C, a thermal sensor immediately activates the fault protection, which shuts down all the outputs except the reference, allowing the device to cool down. Once the device cools down by approximately 15°C, the IC restarts automatically.

Switch Control (MAX8710)

The MAX8710's switch-control block (Figure 6) consists of a high-voltage P-channel MOSFET Q1 between SRC and GON, and a common-source-connected P-channel MOSFET pair Q2 between GON and DRN. The switch-control block is enabled when V_{DLP} goes above V_{REF} / 2. Q1 and Q2 are controlled by CTL and MODE. There are two different modes of operation.

Activate the first mode by connecting MODE to REF. When CTL is logic high, Q1 turns on and Q2 turns off, connecting GON to SRC. When CTL is logic low, Q1 turns off and Q2 turns on, connecting GON to DRN. GON can then be discharged through a resistor connected between DRN and GND or OUTL. Q2 turns off and stops discharging GON when V_{GON} reaches 10 times the voltage on THR.

When V_{MODE} is less than 0.9 x V_{REF}, the switch-control block works in the second mode. The rising edge of V_{CTL} turns on Q1 and turns off Q2, connecting GON to SRC. An internal N-channel MOSFET Q5 between MODE and GND is also turned on to discharge an external capacitor between MODE and GND. The falling edge of V_{CTL} turns off Q5, and an internal 50µA current source starts charging the MODE capacitor. Once V_{MODE} exceeds 0.5 x V_{REF}, the switch-control block turns off Q1 and turns on Q2, connecting GON to DRN. GON can then be discharged through a resistor connected between DRN and GND or OUTL. Q2 turns off and stops discharging GON when V_{GON} reaches 10 times the voltage on THR.

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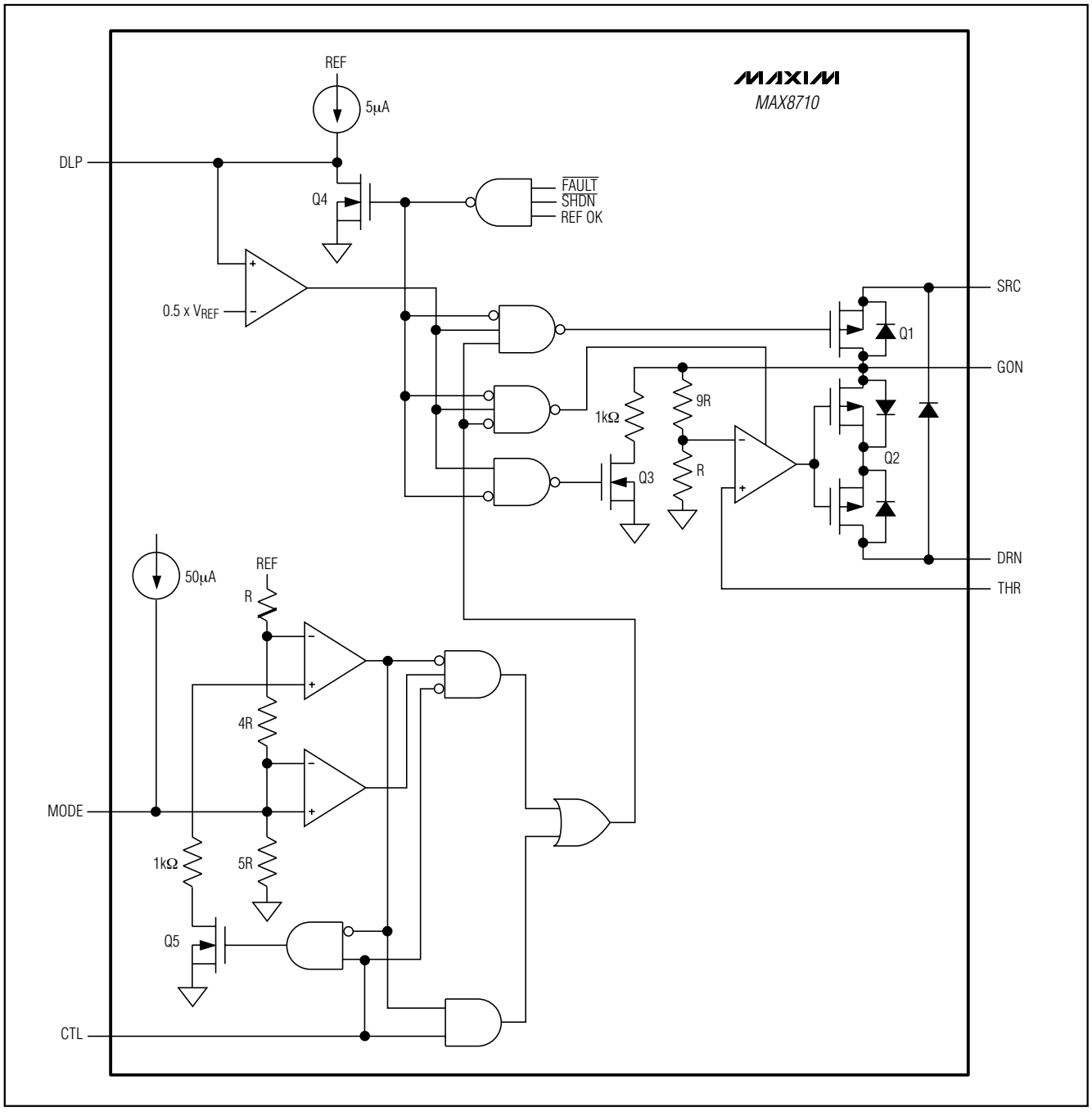

Figure 6. MAX8710 High-Voltage Switch Control

Design Procedure

Linear Regulator

Output-Voltage Selection

Adjust the linear-regulator output voltage by connecting a resistive voltage-divider from the linear-regulator output AVDD to GND with the center tap connected to FBL (Figure 1). Select the lower resistor of the divider R2 in the range of 10kΩ to 50kΩ. Calculate the upper resistor R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{AVDD}}{V_{FBL}} - 1 \right)$$

where V_{FBL} = 2.5V (typ) is the regulation point of the linear regulator.

Input-Capacitor Selection

The linear regulator's output stage consists of a PNP pass transistor. Rapid movements of the input voltage must be avoided since the movement can be coupled into the base of the transistor through the base-to-emitter junction capacitance. The input capacitor reduces the current peaks drawn from the input supply and slows down the input voltage movement. One 10µF ceramic capacitor is used in the *Typical Operating Circuits* (Figure 1, 2, and 3) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance, since the linear regulator typically runs directly from the output of another regulated supply and can operate with less input capacitance.

Output-Capacitor Selection

The output capacitor and its equivalent series resistance (ESR) affect the linear regulator's stability and transient response. The regulator can deliver at least 300mA output current continuously with a 4.7µF output capacitor.

The typical load on the linear regulator for source-driver applications is a large pulsed load, with a peak current of approximately 1A and pulse width of approximately 2µs. The shape of the pulse is close to a triangle, so it is equivalent to a square pulse with 1A height and 1µs pulse width. The total voltage dip during the pulsed load transient also has two components: the ohmic dip due to the output capacitor's ESR, and the capacitive dip caused by discharging the output capacitance:

$$V_{DIP} = V_{DIP(ESR)} + V_{DIP(C)}$$

$$V_{DIP(ESR)} = I_{PULSE} \times R_{ESR}$$

$$V_{DIP(C)} \approx \frac{I_{PULSE} \times t_{PULSE}}{C_{OUT}}$$

where I_{PULSE} is the height of the pulse load, and t_{PULSE} is the pulse width. Higher capacitance and lower ESR result in less voltage dip. The ESR dip can be ignored when using ceramic output capacitors. Calculate the minimum required capacitance for the maximum allowed dip using:

$$C_{OUT(MIN)} \approx \frac{I_{PULSE} \times t_{PULSE}}{V_{DIP(MAX)}}$$

The above equations are "worst-case" and assume that the linear regulator does not react to correct the output voltage during the load pulse. In fact, the regulator is fast enough to partially correct the output voltage, so the actual dip may be smaller, or a smaller capacitor may be acceptable. For the typical load pulse described above, assuming the voltage dip must be limited to 150mV, the minimum output capacitor is:

$$C_{OUT(MIN)} \approx \frac{1A \times 1\mu s}{0.15V} = 6.7\mu F$$

Because the regulator is able to limit the dip somewhat, the circuit of Figure 1 uses a 4.7µF output capacitor. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Feed-Forward Compensation

The output capacitance and equivalent load resistance determine the dominant pole. An internal parasitic capacitance of the regulator creates a second pole. This pole typically occurs at 100kHz, but can vary between 60kHz and 140kHz depending on the process variation. Since the pole occurs after the loop gain crossover, it does not affect the loop stability. However, canceling this pole with an additional zero can improve the load-transient response.

A zero can be added by connecting a feed-forward capacitor (C1) between OUTL and FBL as shown in Figure 1. The frequency of the zero can be calculated with the following equation:

$$f_{ZERO} = \frac{1}{2\pi \times R1 \times C1}$$

where R1 is the upper resistor of the feedback divider. To cancel the second pole, the zero should be placed at or below the frequency of the second pole. Because the frequency of the second pole varies between 60kHz and 140kHz, the zero can be placed between 40kHz and 60kHz.

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Charge-Pump Regulators

Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meets the output requirement.

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_P + V_{SWITCH} - V_{SUPCP}}{V_{INPUT} - 2 \times V_{DIODE}}$$

where n_{POS} is the number of positive charge-pump stages, V_P is the positive charge-pump regulator output, V_{INPUT} is the supply voltage for the charge-pump regulators (V_{SUPCP}, MAX8710 or V_{OUTL}, MAX8711/MAX8712), V_{DIODE} is the forward-voltage drop of the charge-pump diode, and V_{SWITCH} is the voltage drop of the internal switches. Use V_{SWITCH} = 0.3V.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{SWITCH}}{V_{INPUT} - 2 \times V_{DIODE}}$$

where n_{NEG} is the number of negative charge-pump stages and V_{GOFF} is the negative charge-pump regulator output.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{MAIN} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to another available supply, such as a 5V supply. If the first charge-pump stage is powered from 5V, then the above equations become:

$$n_{POS} = \frac{V_P + V_{SWITCH} - 5V}{V_{INPUT} - 2 \times V_{DIODE}}$$

$$n_{NEG} = \frac{-V_{GOFF} + V_{SWITCH} + 5V}{V_{INPUT} - 2 \times V_{DIODE}}$$

Output Voltage Selection

Adjust the positive charge-pump-regulator output voltage by connecting a resistive voltage-divider from the regulator output V_P to GND with the center tap connected to FBP (Figure 1). Select the lower resistor of divider R4 in the range of 10kΩ to 50kΩ. Calculate upper resistor R3 with the following equation:

$$R3 = R4 \times \left(\frac{V_P}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 2.5V (typ) is the regulation point of the positive charge-pump regulator.

Adjust the negative charge-pump-regulator output voltage by connecting a resistive voltage-divider from the negative charge-pump output V_{GOFF} to REF with the center tap connected to FBN (Figure 1). Select R6 in the 20kΩ to 100kΩ range. Calculate R5 with the following equation:

$$R5 = R6 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{REF} = 5V and V_{FBN} = 250mV is the regulation point of the negative charge-pump regulator.

Flying Capacitor

Increasing the flying-capacitor (C_X) value lowers the effective source impedance and increases the output-current capability of the charge pump. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{INPUT}$$

where n is the stage number in which the flying capacitor is used, and V_{INPUT} is the supply voltage for the charge-pump regulators (V_{SUPCP}, MAX8710 or V_{OUTL}, MAX8711/MAX8712).

Charge-Pump Input Capacitor

Use an input capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect the capacitor directly to PGND.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} \geq \frac{I_{LOAD\_CP}}{2f_{OSC}V_{RIPPLE\_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the desired peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diode

Use low-cost silicon switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating.

Applications Information

External Transistor for Higher Current or Power Dissipation

The load current and the voltage difference between the input and output determine the linear regulator's power dissipation as shown in the following equation:

$$P_{DISSIPATION} = (V_{INL} - V_{OUTL}) \times I_{OUTL}$$

For some applications, the input voltage to the linear regulator is from a 19V adapter. To make a 10V output, the voltage across the pass transistor is 9V. In this case, the regulator's power dissipation may exceed the dissipation limit that the package can handle. In some other applications, the load current may be much higher than the regulator's guaranteed 300mA output current.

The solution for such applications is to connect an external PNP transistor with the internal PNP transistor in a Darlington configuration as shown in Figure 7. The external pass transistor must be able to handle most of the power dissipation since most of the load current flows through it. On the other hand, the power dissipated in the internal pass transistor is very low. The current-limit circuit will not work if an external pass transistor is used because the linear regulator only senses the current of the internal pass transistor.

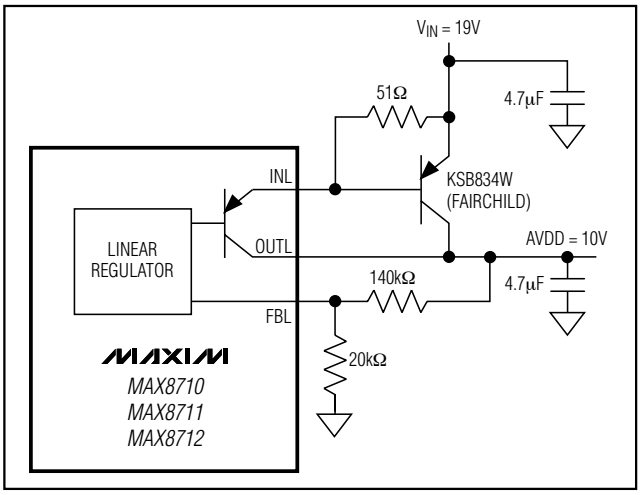


Figure 7. High-Power Linear Regulator

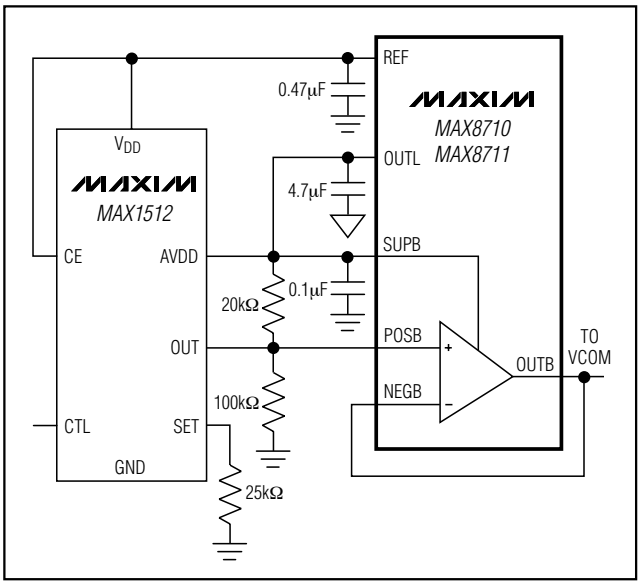


Figure 8. Using the MAX1512 to Adjust the VCOM Buffer Output

Using the MAX1512 VCOM Calibrator to Adjust the Buffer Output

The operational amplifier is typically used as the VCOM buffer in TFT LCD panels. The output voltage of the VCOM buffer can be adjusted using the MAX1512, which is an EEPROM-programmable VCOM calibrator, using the circuit shown in Figure 8. Refer to the MAX1512 data sheet for details.

Low-Cost Linear-Regulator LCD Panel Power Supplies

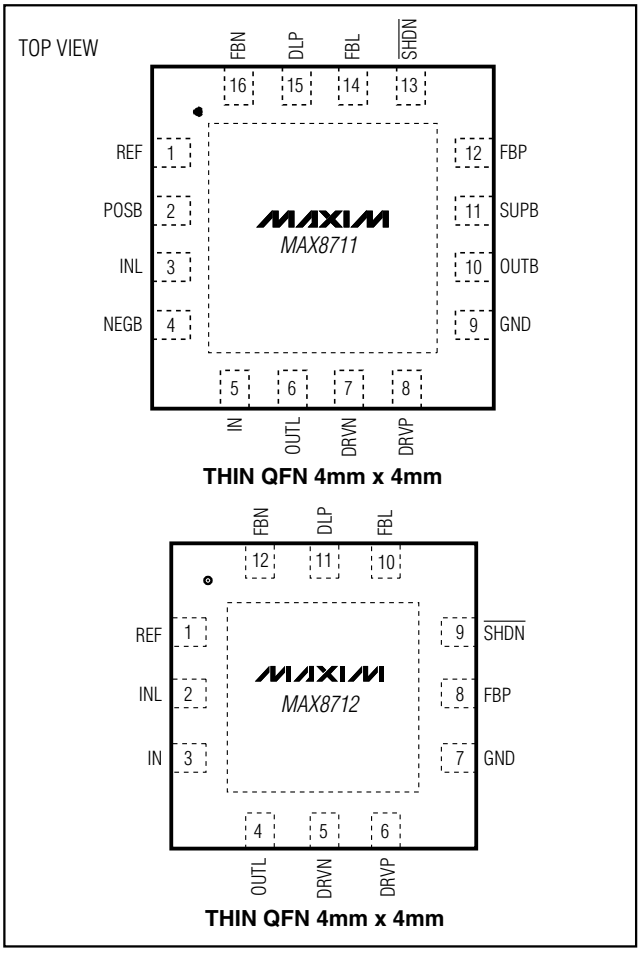
PC Board Layout Guidelines

Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

1) Create a power ground island consisting of the linear-regulator input and output-capacitor ground connections, the GND pin, and the capacitor ground connections for the charge-pump regulators. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency. Create an analog ground island consisting of all the feedback-divider ground connections, the operational-amplifier divider ground connection, the REF capacitor ground connection, the MODE capacitor ground connection, the DLP capacitor ground connection, and the device's exposed backside pad. Connect the analog ground island and the power ground island by connecting the GND pin directly to the exposed backside pad. Make no other connections between these separate ground islands.
2) Place all feedback voltage-divider resistors as close to their respective feedback pins as possible. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up noise from the switching nodes of the charge pumps. Avoid running any feedback trace near these switching nodes.
3) Place IN, INL, SUPB, SUPCP, and REF pin bypass capacitors close to the IC. The ground connection of the IN bypass capacitor should be connected directly to the GND pin with a wide trace.
4) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
5) Minimize the size of the switching nodes (DRVP and DRVN). Keep the switching nodes away from feedback nodes (FBL, FBP, and FBN) and the analog ground. Use DC traces as a shield if necessary.

Refer to the MAX8710 evaluation kit for an example of proper board layout.

Pin Configurations (continued)



Chip Information

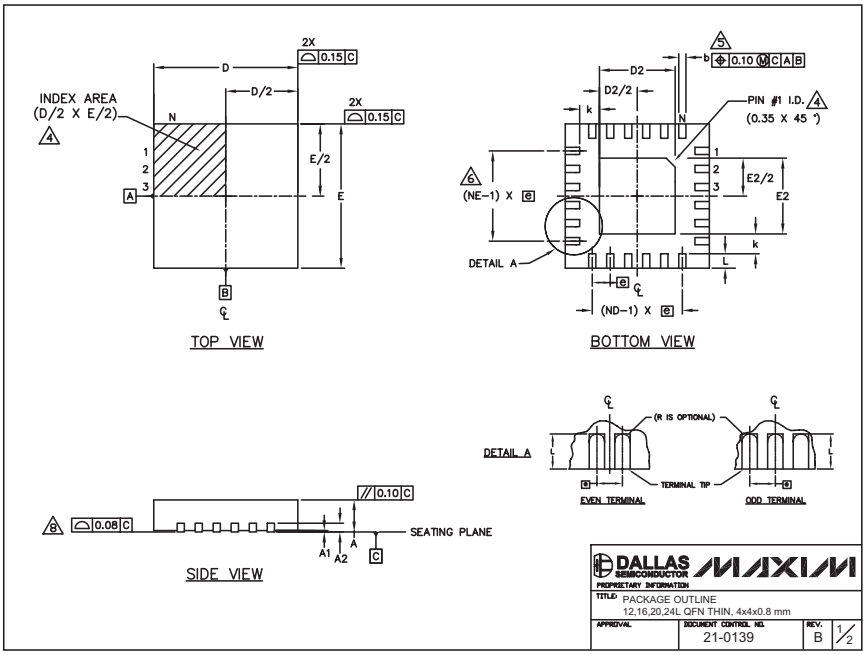
TRANSISTOR COUNT: 3946

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 1/2

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 2/2

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