19-2864; Rev 1; 8/03

MAXIM

Programmable DC-Balance 21-Bit Deserializers

General Description

The MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 deserialize three LVDS serial data inputs into 21 single-ended LVCMOS/LVTTL outputs. A parallel rate LVDS clock received with the LVDS data streams provides timing for deserialization. The outputs have a separate supply, allowing 1.8V to 5V output logic levels.

The MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 feature programmable DC balance, which allows isolation between a serializer and deserializer using AC-coupling. A deserializer decodes data transmitted by a MAX9209/MAX9211/MAX9213/MAX9215 serializer.

The MAX9210/MAX9212/MAX9214/MAX9216 have rising-edge output strobes, and when DC balance is not programmed, are compatible with non-DC-balanced 21-bit deserializers such as the DS90CR216A and DS90CR218A. The MAX9220/MAX9222 have falling-edge output strobes.

Two frequency versions and two DC balance default conditions are available for maximum replacement flexibility and compatibility with popular non-DC-balanced deserializers. The transition time of the single-ended outputs is increased on the low-frequency version parts (MAX9210/MAX9212/MAX9220) for reduced EMI.

The MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 are available in TSSOP and space-saving QFN packages, and operate over the -40°C to +85°C temperature range.

Applications

Automotive Navigation Systems

Automotive DVD Entertainment Systems

Digital Copiers

Laser Printers

Functional Diagram and Pin Configurations appear at end of data sheet.

Features

- **Programmable DC Balance or Non-DC Balance**
- **DC Balance Allows AC-Coupling for Wider Input Common-Mode Voltage Range**
- **As Low as 8MHz Operation (MAX9210/MAX9212/MAX9220)**
- **Falling-Edge Output Strobe (MAX9220/MAX9222)**
- **Slower Output Transitions for Reduced EMI (MAX9210/MAX9212/MAX9220)**
- **High-Impedance Outputs when $\overline{\text{PWRDWN}}$ is Low Allow Output Busing**
- **Pin Compatible with DS90CR216A/DS90CR218A (MAX9210/MAX9212/MAX9214/MAX9216)**
- **Fail-Safe Inputs in Non-DC-Balanced Mode**
- **5V Tolerant $\overline{\text{PWRDWN}}$ Input**
- **PLL Requires No External Components**
- **Up to 1.785Gbps Throughput**
- **Separate Output Supply Pins Allow Interface to 1.8V, 2.5V, 3.3V, and 5V Logic**
- **LVDS Inputs Meet IEC 61000-4-2 Level 4 ESD Requirements**
- **LVDS Inputs Conform to ANSI TIA/EIA-644 LVDS Standard**
- **Low-Profile 48-Lead TSSOP and Space-Saving QFN Packages**
- **+3.3V Main Power Supply**
- **-40°C to +85°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9210ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9210EUM*	-40°C to +85°C	48 TSSOP
MAX9212ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9212EUM*	-40°C to +85°C	48 TSSOP
MAX9214ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9214EUM	-40°C to +85°C	48 TSSOP
MAX9216ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9216EUM*	-40°C to +85°C	48 TSSOP
MAX9220ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9220EUM*	-40°C to +85°C	48 TSSOP
MAX9222ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9222EUM	-40°C to +85°C	48 TSSOP

**Future product—contact factory for availability.*
***EP = Exposed pad.*

Programmable DC-Balance 21-Bit Deserializers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +4.0V
V_{CCO} to GND.....-0.5V to +6.0V
RxIN_, RxCLK IN_ to GND .....-0.5V to +4.0V
$\overline{PWRDWN}$ to GND .....-0.5V to +6.0V
DCB/NC to GND.....-0.5V to (V_{CC} + 0.5V)
RxOUT_, RxCLK OUT to GND .....-0.5V to (V_{CCO} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
48-Pin TSSOP (derate 16mW/°C above +70°C)..... 1282mW
48-Lead Thin QFN
(derate 26.3mW/°C above +70°C) 2105mW
Storage Temperature Range.....-65°C to +150°C
Junction Temperature .....+150°C
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND .....±5kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF) Level 4
Contact Discharge LVDS Inputs (RxIN_, RxCLK IN_)
to GND .....±8kV
Air Discharge LVDS Inputs (RxIN_, RxCLK IN_)
to GND .....±15kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, V_{CCO} = +3.0V to +5.5V, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS ($\overline{PWRDWN}$, DCB/NC)						
High-Level Input Voltage	V_{IH}	$\overline{PWRDWN}$	2.0		5.5	V
		DCB/NC	2.0		V_{CC} + 0.3	
Low-Level Input Voltage	V_{IL}		-0.3		+0.8	V
Input Current	I_{IN}	V_{IN} = high or low, $\overline{PWRDWN}$ = high or low	-20		+20	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-1.5	V
SINGLE-ENDED OUTPUTS (RxOUT_, RxCLK OUT)						
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA	V_{CCO} - 0.1			V
		I_{OH} = -2mA	V_{CCO} - 0.25			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA			0.1	V
		I_{OL} = 2mA			0.2	
High-Impedance Output Current	I_{OZ}	$\overline{PWRDWN}$ = low, $V_{OUT\_}$ = -0.3V to (V_{CCO} + 0.3V)	-20		+20	µA
Output Short-Circuit Current **Note:** Short one output at a time.	I_{OS}	V_{CCO} = 3.0V to 3.6V, V_{OUT} = 0V	-10		-40	mA
		V_{CCO} = 4.5V to 5.5V, V_{OUT} = 0V	-28		-75	
LVDS INPUTS						
Differential Input High Threshold	V_{TH}				50	mV
Differential Input Low Threshold	V_{TL}		-50			mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, V_{CCO} = +3.0V to +5.5V, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	I_{IN+}, I_{IN-}	$\overline{PWRDWN}$ = high or low		-25		+25	µA
Power-Off Input Current	I_{INO+}, I_{INO-}	V_{CC} = V_{CCO} = 0V or open, DCB/NC, $\overline{PWRDWN}$ = 0V or open		-25		+25	µA
Input Resistor 1	R_{IN1}	$\overline{PWRDWN}$ = high or low (Figure 1)		42		78	kΩ
		V_{CC} = V_{CCO} = 0V or open (Figure 1)					
Input Resistor 2	R_{IN2}	$\overline{PWRDWN}$ = high or low (Figure 1)		246		410	kΩ
		V_{CC} = V_{CCO} = 0V or open (Figure 1)					
POWER SUPPLY							
Worst-Case Supply Current	I_{CCW}	C_L = 8pF, worst-case pattern, DC-balanced mode; V_{CC} = V_{CCO} = 3.0V to 3.6V, Figure 2	16MHz		52	63	mA
			34MHz		86	106	
			66MHz		152	177	
		C_L = 8pF, worst-case pattern, non-DC-balanced mode; V_{CC} = V_{CCO} = 3.0V to 3.6V, Figure 2	20MHz		53	64	
			33MHz		72	85	
			40MHz		81	99	
			66MHz		127	149	
			85MHz		159	186	
Power-Down Supply Current	I_{CCZ}	$\overline{PWRDWN}$ = low				50	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CCO} = +3.0V to 3.6V, 100mV_{P-P} at 200kHz supply noise, C_L = 8pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = 25°C.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Rise Time	CLHT	0.1 x V_{CCO} to 0.9 x V_{CCO}, Figure 3		2.2	3.15	3.9	ns
Output Fall Time	CHLT	0.9 x V_{CCO} to 0.1 x V_{CCO}, Figure 3		1.3	2.12	2.9	ns
RxIN Skew Margin	RSKM	DC-balanced mode, Figure 4 (Note 6)	16MHz	2560	3137		ps
			34MHz	900	1327		
			66MHz	330	685		
		Non-DC-balanced mode, Figure 4 (Note 6)	20MHz	2500	3300		
			40MHz	960	1448		
			85MHz	330	685		

Programmable DC-Balance 21-Bit Deserializers

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CCO} = +3.0V to 3.6V, 100mV$_{P-P}$ at 200kHz supply noise, C_L = 8pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = 25°C.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RxCLK OUT High Time	RCOH	Figures 5a, 5b	0.35 x RCOP	0.4 x RCOP		ns
RxCLK OUT Low Time	RCOL	Figures 5a, 5b	0.35 x RCOP	0.44 x RCOP		ns
RxOUT Setup to RxCLK OUT	RSRC	Figures 5a, 5b	0.30 x RCOP	0.35 x RCOP		ns
RxOUT Hold from RxCLK OUT	RHRC	Figures 5a, 5b	0.45 x RCOP	0.48 x RCOP		ns
RxCLK IN to RxCLK OUT Delay	RCCD	Figures 6a, 6b	4.9	6.17	8.1	ns
Deserializer Phase-Locked Loop Set	RPLLS	Figure 7			32800 x RCIP	ns
Deserializer Power-Down Delay	RPDD	Figure 8			100	ns

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} and V_{TL}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

Note 4: C_L includes probe and test jig capacitance.

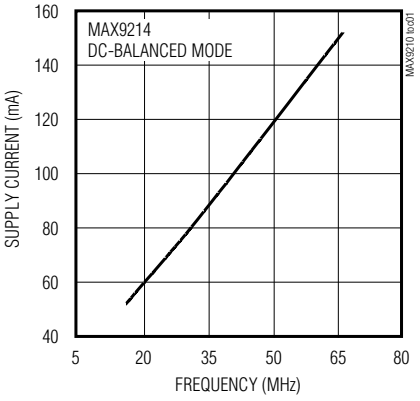
Note 5: RCIP is the period of RxCLK IN. RCOP is the period of RxCLK OUT. RCIP = RCOP.

Note 6: RSKM measured with ≤150ps cycle-to-cycle jitter on RxCLK IN.

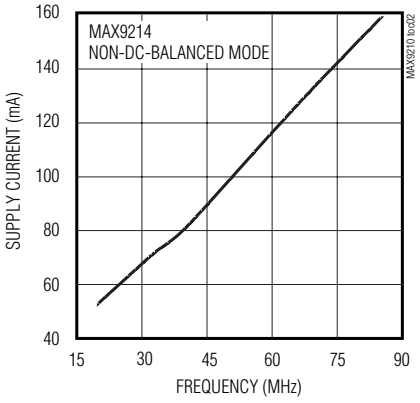
Typical Operating Characteristics

(V_{CC} = V_{CCO} = +3.3V, C_L = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.)

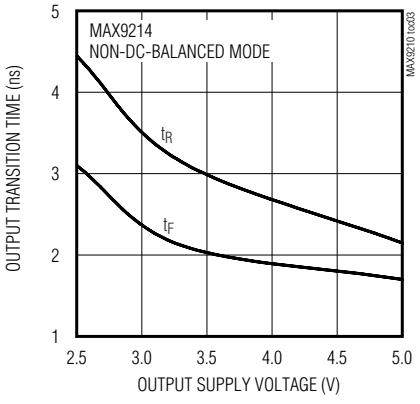
WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY



WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY



OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE (V_{CCO})



Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1, 2, 4, 5, 45, 46, 47	39, 40, 41, 43, 44, 46, 47	RxOUT14–RxOUT20	Channel 2 Single-Ended Outputs
3, 25, 32, 38, 44	19, 26, 32, 38, 45	GND	Ground
6	48	DCB/NC	LVTTL/LVCMOS DC-Balance Programming Input: MAX9210: pulled up to V_{CC} MAX9212: pulled down to GND MAX9214: pulled up to V_{CC} MAX9216: pulled down to GND MAX9220: pulled up to V_{CC} MAX9222: pulled up to V_{CC} See Table 1.
7, 13, 18	1, 7, 12	LVDS GND	LVDS Ground
8	2	RxIN0-	Inverting Channel 0 LVDS Serial Data Input
9	3	RxIN0+	Noninverting Channel 0 LVDS Serial Data Input
10	4	RxIN1-	Inverting Channel 1 LVDS Serial Data Input
11	5	RxIN1+	Noninverting Channel 1 LVDS Serial Data Input
12	6	LVDS V_{CC}	LVDS Supply Voltage
14	8	RxIN2-	Inverting Channel 2 LVDS Serial Data Input
15	9	RxIN2+	Noninverting Channel 2 LVDS Serial Data Input
16	10	RxCLK IN-	Inverting LVDS Parallel Rate Clock Input
17	11	RxCLK IN+	Noninverting LVDS Parallel Rate Clock Input
19, 21	13, 15	PLL GND	PLL Ground
20	14	PLL V_{CC}	PLL Supply Voltage
22	16	$\overline{PWRDWN}$	5V Tolerant LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND. Outputs are high impedance when $\overline{PWRDWN}$ = low or open.
23	17	RxCLK OUT	Parallel Rate Clock Single-Ended Output. MAX9210/MAX9212/MAX9214/MAX9216, rising edge strobe. MAX9220/MAX9222, falling edge strobe.
24, 26, 27, 29, 30, 31, 33	18, 20, 21, 23, 24, 25, 27	RxOUT0–RxOUT6	Channel 0 Single-Ended Outputs
28, 36, 48	22, 30, 42	V_{CCO}	Output Supply Voltage
34, 35, 37, 39, 40, 41, 43	28, 29, 31, 33, 34, 35, 37	RxOUT7–RxOUT13	Channel 1 Single-Ended Outputs
42	36	V_{CC}	Digital Supply Voltage
—	EP	EP	Exposed Paddle. Solder to ground.

Programmable DC-Balance 21-Bit Deserializers

Table 1. DC-Balance Programming

DEVICE	DCB/NC	OUTPUT STROBE EDGE	OPERATING MODE	OPERATING FREQUENCY (MHz)
MAX9210	High or open	Rising	DC balanced	8 to 34
	Low		Non-DC balanced	10 to 40
MAX9212	High	Rising	DC balanced	8 to34
	Low or open		Non-DC balanced	10 to 40
MAX9214	High or open	Rising	DC balanced	16 to 66
	Low		Non-DC balanced	20 to 85
MAX9216	High	Rising	DC balanced	16 to 66
	Low or open		Non-DC balanced	20 to 85
MAX9220	High or open	Falling	DC balanced	8 to 34
	Low		Non-DC balanced	10 to 40
MAX9222	High or open	Falling	DC balanced	16 to 66
	Low		Non-DC balanced	20 to 85

Detailed Description

The MAX9210/MAX9212/MAX9220 operate at a parallel clock frequency of 8MHz to 34MHz in DC-balanced mode and 10MHz to 40MHz in non-DC-balanced mode. The MAX9214/MAX9216/MAX9222 operate at a parallel clock frequency of 16MHz to 66MHz in DC-balanced mode and 20MHz to 85MHz in non-DC-balanced mode. The transition times of the single-ended outputs are increased on the MAX9210/MAX9212/MAX9220 for reduced EMI.

DC-balanced or non-DC-balanced operation is controlled by the DCB/NC pin (see Table 1 for DCB/NC default settings and operating modes). In non-DC-balanced mode, each channel deserializes 7 bits every cycle of the parallel clock. In DC-balanced mode, 9 bits are deserialized every clock cycle (7 data bits + 2 DC-balance bits). The highest data rate in DC-balanced mode for the MAX9214, MAX9216, and MAX9222 is 66MHz x 9 = 594Mbps. In non-DC-balanced mode, the maximum data rate is 85MHz x 7 = 595Mbps.

DC Balance

Data coding by the MAX9209/MAX9211/MAX9213/MAX9215 serializers (which are companion devices to the MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 deserializers) limits the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary 1 transmitted and -1 is assigned to each binary 0 transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the data channels is 10. At most, 10 more zeros than ones, or 10 more ones than zeros, are transmitted. The maximum DSV for the clock

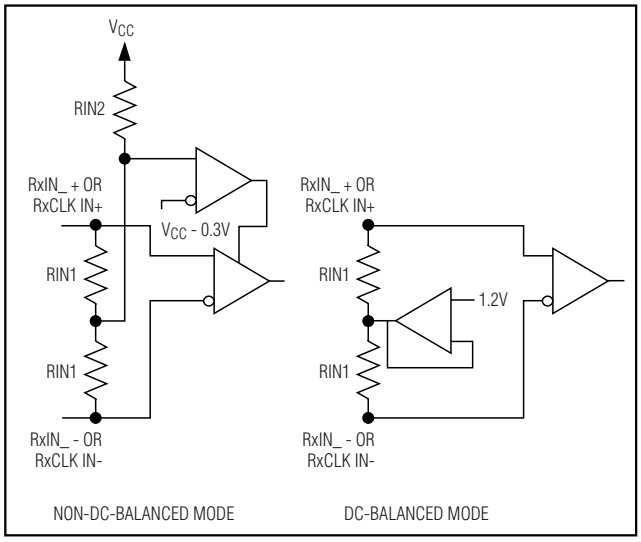


Figure 1. LVDS Input Circuits

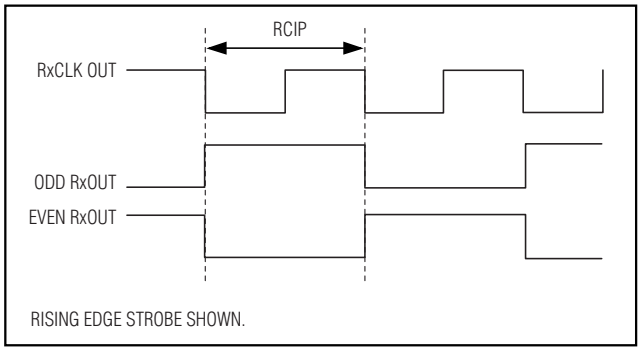


Figure 2. Worst-Case Test Pattern

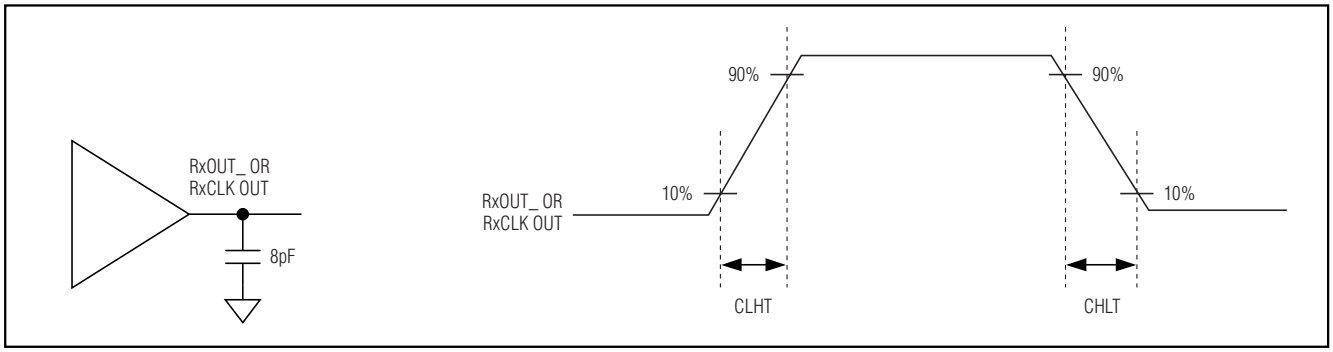


Figure 3. Output Load and Transition Times

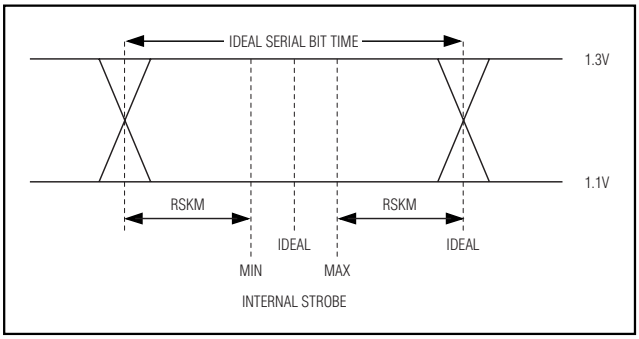


Figure 4. LVDS Receiver Input Skew Margin

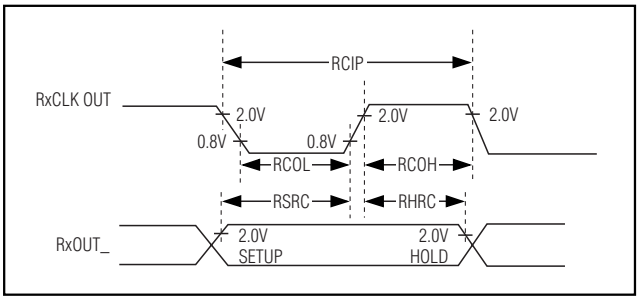


Figure 5a. Rising-Edge Output Setup/Hold and High/Low Times

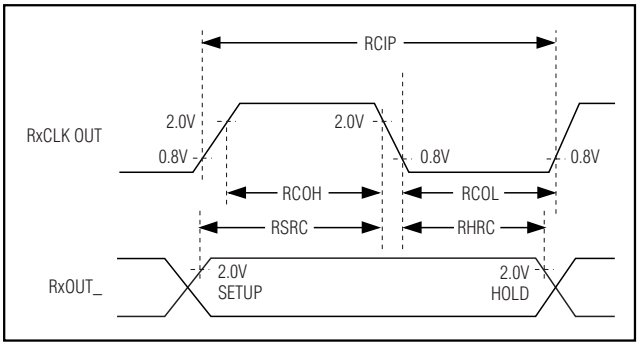


Figure 5b. Falling-Edge Output Setup/Hold and High/Low Times

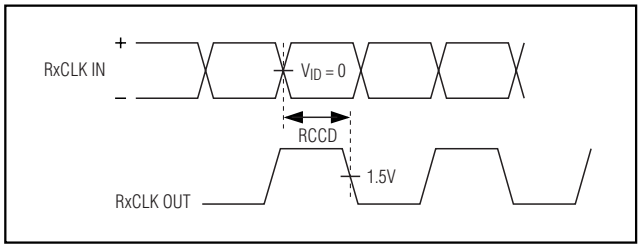


Figure 6a. Rising-Edge Clock-IN to Clock-OUT Delay

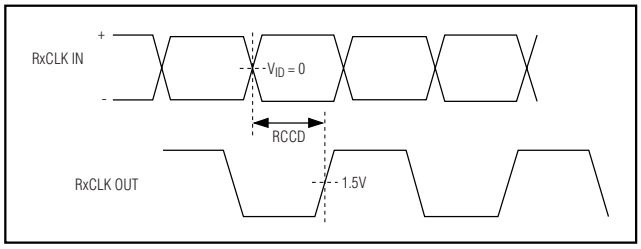


Figure 6b. Falling-Edge Clock-IN to Clock-OUT Delay

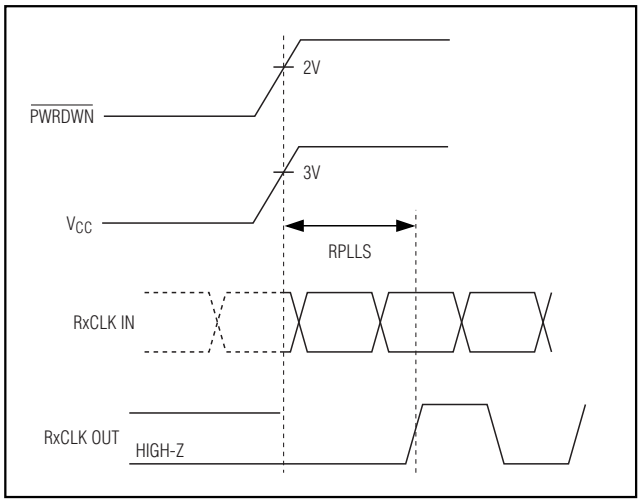


Figure 7. Phase-Locked Loop Set Time

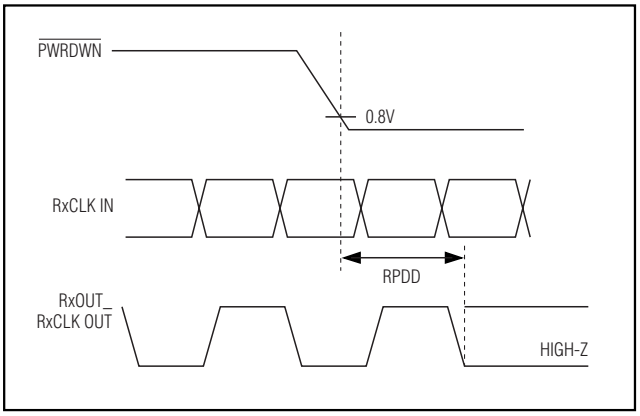


Figure 8. Power-Down Delay

channel is five. Limiting the DSV and choosing the correct coupling capacitors maintains differential signal amplitude and reduces jitter due to droop on AC-coupled links.

To obtain DC balance on the data channels, the serializer parallel data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel input data bits to indicate to the MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 deserializers whether the data bits are inverted (see Figures 9 and 10). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9, which maintain DC balance.

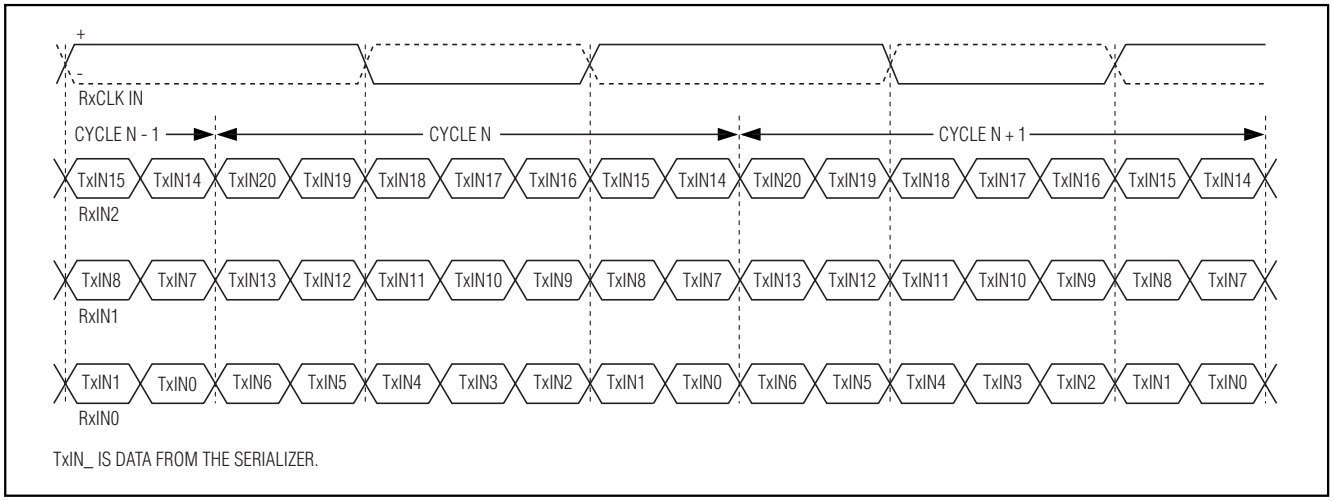


Figure 9. Deserializer Serial Input in Non-DC-Balanced Mode

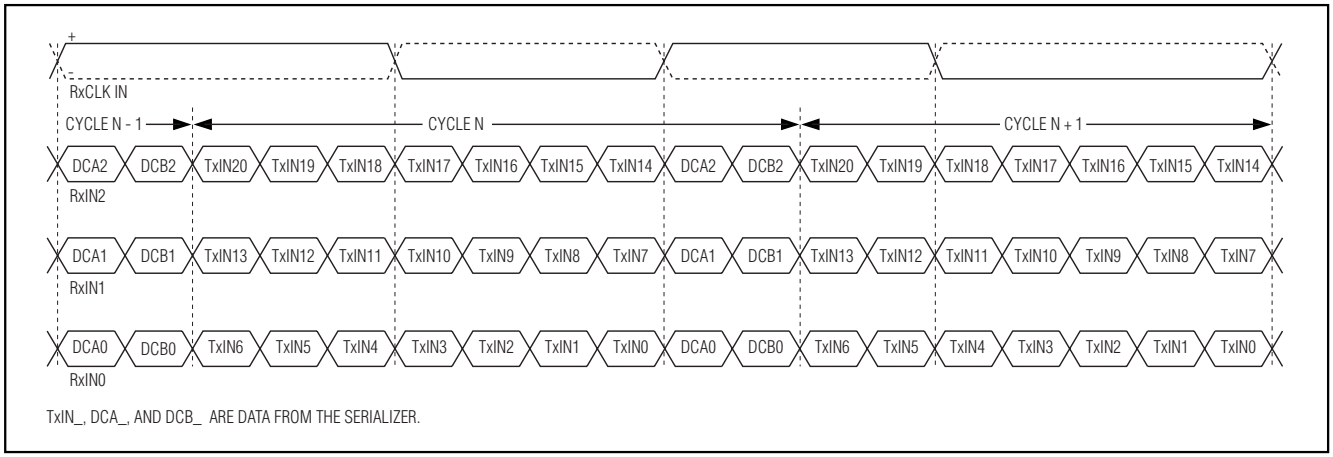


Figure 10. Deserializer Serial Input in DC-Balanced Mode

AC-Coupling Benefits

Bit errors experienced with DC-coupling can be eliminated by increasing the receiver common-mode voltage range by AC-coupling. AC-coupling increases the common-mode voltage range of an LVDS receiver to nearly the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on an offset voltage of 1.25V, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0V to 2.4V, allowing approximately ±1V common-mode difference between the driver and receiver on a DC-coupled link (2.4V - 1.425V = 0.975V and 1.075V - 0V = 1.075V). Common-mode voltage differences may be due to ground potential variation or common-mode noise. If there is more than ±1V of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

Applications Information

Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols causes signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

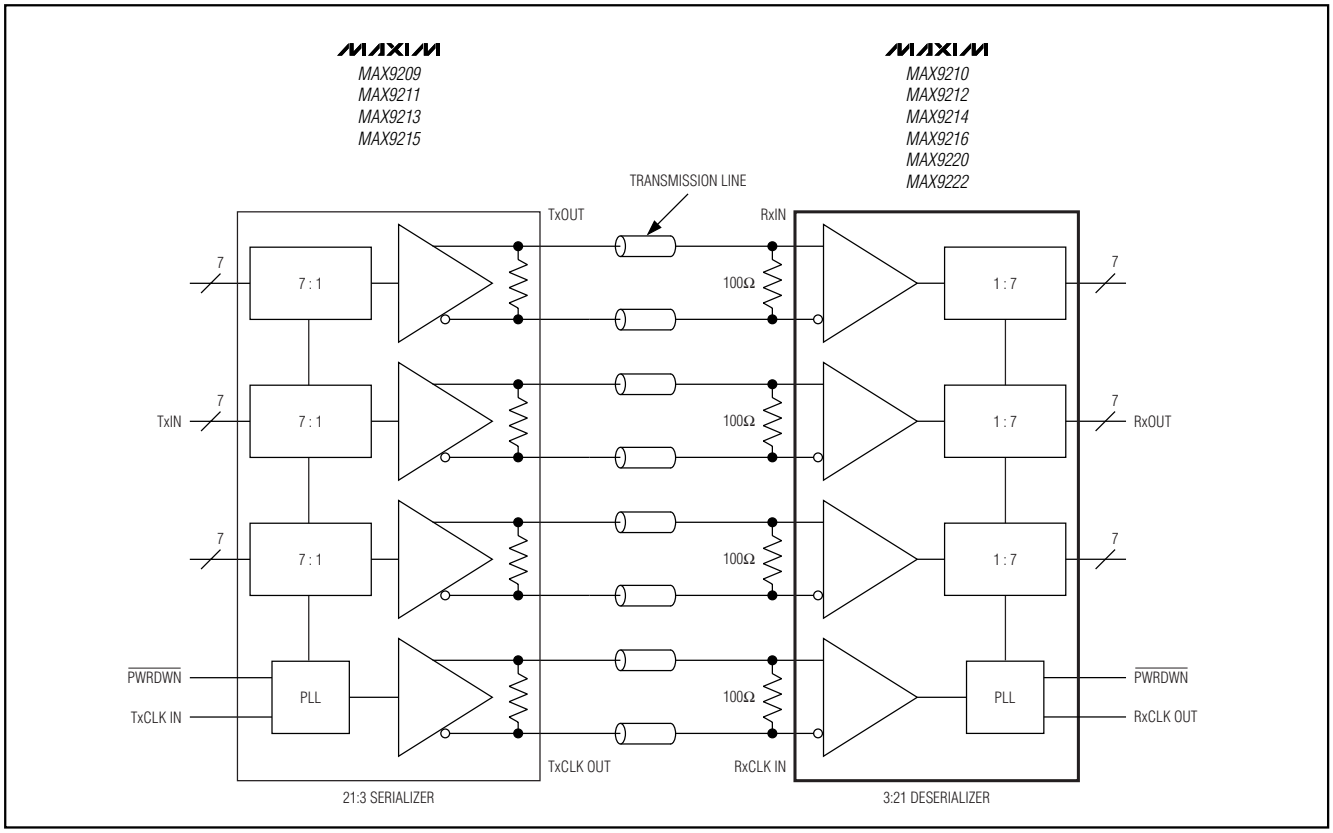


Figure 11. DC-Coupled Link, Non-DC-Balanced Mode

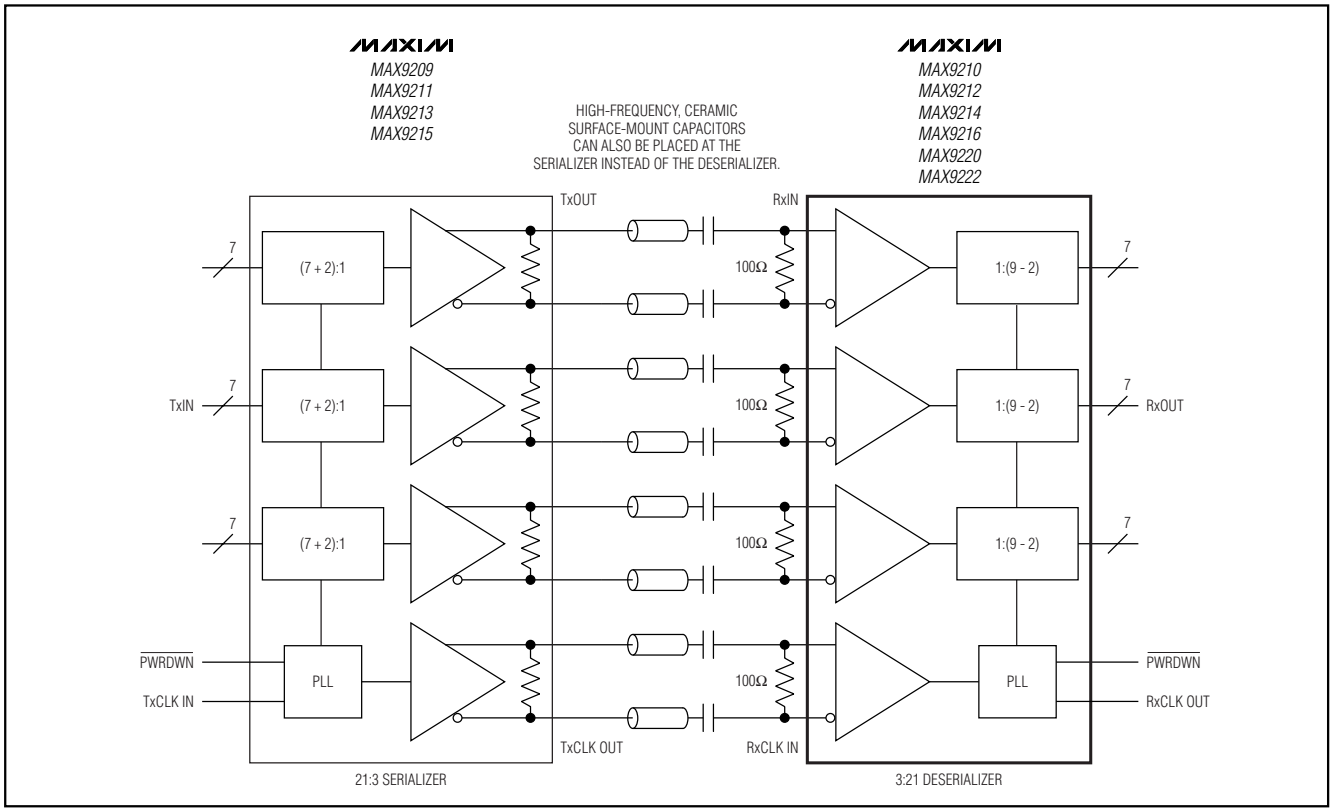


Figure 12. Two Capacitors per Link, AC-Coupled, DC-Balanced Mode

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor (R_T), the LVDS driver output resistor (R_O), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series capacitors is (C x (R_T + R_O))/2 (Figure 12). The RC time constant for four equal-value series capacitors is (C x (R_T + R_O))/4 (Figure 13).

R_T is required to match the transmission line impedance (usually 100Ω) and R_O is determined by the LVDS driver design (the minimum differential output resistance of 78Ω for the MAX9209/MAX9211/MAX9213/MAX9215 serializers is used in the following example). This leaves the capacitor selection to change the system time constant.

In the following example, the capacitor value for a droop of 2% is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = - (2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 1)}$$

where:
C = AC-coupling capacitor (F)
t_B = bit time (s)
DSV = digital sum variation (integer)
ln = natural log
D = droop (% of signal amplitude)
R_T = termination resistor (Ω)
R_O = output resistance (Ω)

Equation 1 is for two series capacitors (Figure 12). The bit time (t_B) is the period of the parallel clock divided by 9. The DSV is 10. See equation 3 for four series capacitors (Figure 13).

The capacitor for 2% maximum droop at 8MHz parallel rate clock is:

$$C = - (2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O))$$

$$C = - (2 \times 13.9ns \times 10) / (\ln (1 - 0.02) \times (100\Omega + 78\Omega))$$

$$C = 0.0773\mu F$$

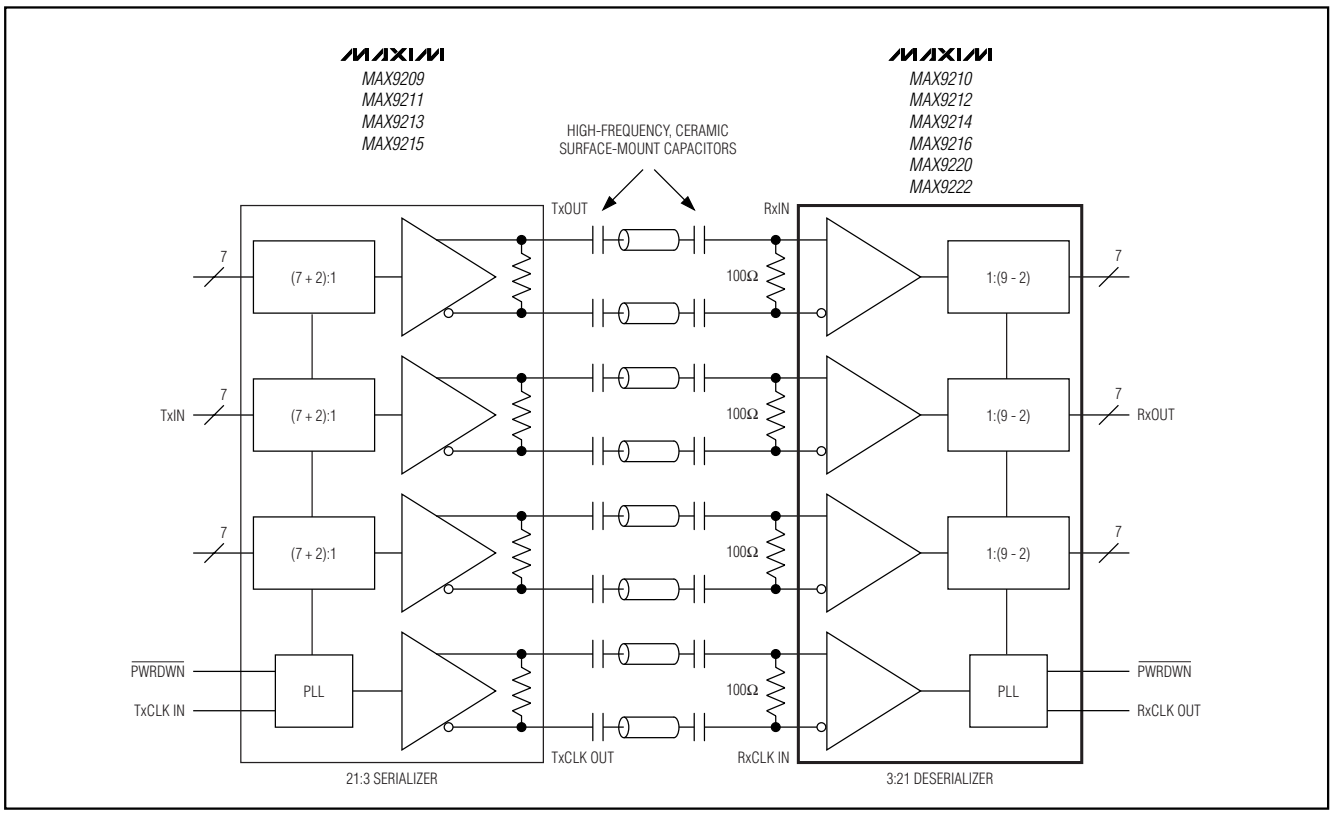


Figure 13. Four Capacitors per Link, AC-Coupled, DC-Balanced Mode

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \text{ (Eq 2)}$$

where:
t_J = jitter (s)
t_T = transition time (s) (0% to 100%)
D = droop (% of signal amplitude)

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1ns \times 0.02$$

$$t_J = 20ps$$

The transition time in a real system depends on the frequency response of the cable driven by the serializer. The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 13) is:

$$C = - (4 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \text{ (Eq 3)}$$

Fail-Safe

The MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 have fail-safe LVDS inputs in non-DC-balanced mode (Figure 1). Fail-safe drives the outputs low when the corresponding LVDS input is open, undriven and shorted, or undriven and parallel terminated. The fail-safe on the LVDS clock input drives all outputs low. Fail-safe does not operate in DC-balanced mode.

Input Bias and Frequency Detection

In DC-balanced mode, the inverting and noninverting LVDS inputs are internally connected to +1.2V through 42kΩ (min) to provide biasing for AC-coupling (Figure 1). A frequency-detection circuit on the clock input detects when the input is not switching, or is switching at low frequency. In this case, all outputs are driven low. To prevent switching due to noise when the clock input is not driven, bias the clock input to differential +15mV by connecting a 10kΩ ±1% pullup resistor between the noninverting input and V_{CC}, and a 10kΩ ±1% pulldown resistor between the inverting input and ground. These

Programmable DC-Balance 21-Bit Deserializers

bias resistors, along with the 100Ω ±1% tolerance termination resistor, provide +15mV of differential input. However, the +15mV bias causes degradation of RSKM proportional to the slew rate of the clock input. For example, if the clock transitions 250mV in 500ps, the slew rate of 0.5mV/ps reduces RSKM by 30ps.

Unused LVDS Data Inputs

In non-DC-balanced mode, leave unused LVDS data inputs open. In non-DC balanced mode, the input failsafe circuit drives the corresponding outputs low and no pullup or pulldown resistors are needed. In DC-balanced mode, at each unused LVDS data input, pull the inverting input up to V_{CC} using a 10kΩ resistor, and pull the noninverting input down to ground using a 10kΩ resistor. Do not connect a termination resistor. The pullup and pulldown resistors drive the corresponding outputs low and prevent switching due to noise.

$\overline{PWRDWN}$

Driving $\overline{PWRDWN}$ low puts the outputs in high impedance, stops the PLL, and reduces supply current to 50µA or less. Driving $\overline{PWRDWN}$ high drives the outputs low until the PLL locks. The outputs of two deserializers can be bused to form a 2:1 mux with the outputs controlled by $\overline{PWRDWN}$. Wait 100ns between disabling one deserializer (driving $\overline{PWRDWN}$ low) and enabling the second one (driving $\overline{PWRDWN}$ high) to avoid contention of the bused outputs.

Input Clock and PLL Lock Time

There is no required timing sequence for the application or reapplication of the parallel rate clock (RxCLK IN) relative to $\overline{PWRDWN}$, or to a power-supply ramp for proper PLL lock. The PLL lock time is set by an internal counter. The maximum time to lock is 32,800 clock periods. Power and clock should be stable to meet the lock time specification. When the PLL is locking, the outputs are low.

Power-Supply Bypassing

There are separate on-chip power domains for digital circuits, outputs, PLL, and LVDS inputs. Bypass each V_{CC}, V_{CCO}, PLL V_{CC}, and LVDS V_{CC} pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Keep the LVTTL/LVCMOS outputs and LVDS input signals separated to prevent crosstalk. A four-layer PC board with separate layers for power, ground, LVDS inputs, and digital signals is recommended.

IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard specifies ESD tolerance for electronic systems. The IEC 61000-4-2 model (Figure 14) specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9210/MAX9212/MAX9214/MAX9216/MAX9220/MAX9222 LVDS inputs are rated for IEC 61000-4-2 level 4 (±8kV contact discharge and ±15kV air discharge). IEC 61000-4-2 discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor. The HBM (Figure 15) specifies a 100pF capacitor that is discharged into the device through a 1.5kΩ resistor. All pins are rated for ±5kV HBM.

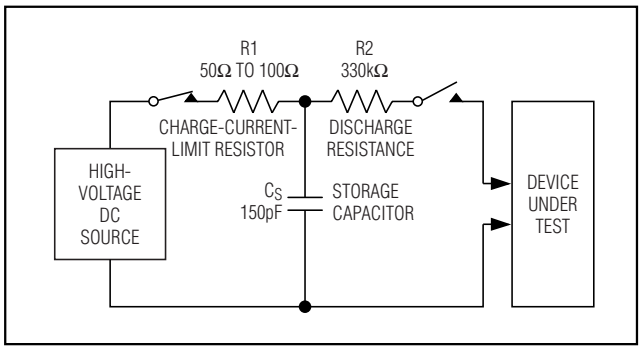


Figure 14. IEC 61000-4-2 Contact Discharge ESD Test Circuit

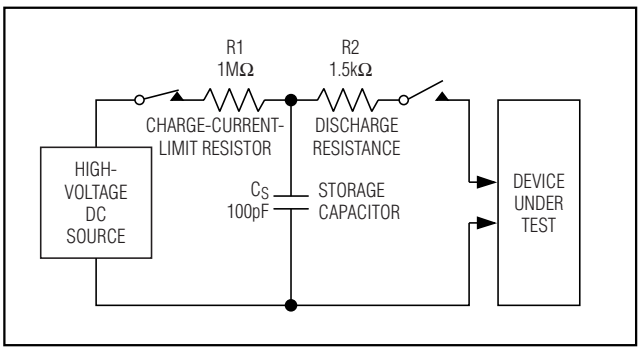


Figure 15. Human Body ESD Test Circuit

5V Tolerant Input

$\overline{PWRDWN}$ is 5V tolerant and is internally pulled down to GND. DCB/NC is not 5V tolerant. The input voltage range for DCB/NC is nominally ground to V_{CC}. Normally, DCB/NC is connected to V_{CC} or ground.

Skew Margin (RSKM)

Skew margin (RSKM) is the time allowed for degradation of the serial data sampling setup and hold times by sources other than the deserializer. The deserializer sampling uncertainty is accounted for and does not need to be subtracted from RSKM. The main outside contributors of jitter and skew that subtract from RSKM are interconnect intersymbol interference, serializer pulse position uncertainty, and pair-to-pair path skew.

V_{CCO} Output Supply and Power Dissipation

The outputs have a separate supply (V_{CCO}) for interfacing to systems with 1.8V to 5V nominal input logic levels. The *DC Electrical Characteristics* table gives the maximum supply current for V_{CCO} = 3.6V with 8pF load at several switching frequencies with all outputs switching in the worst-case switching pattern. The approximate incremental supply current for V_{CCO} other than 3.6V **with the same 8pF** load and worst-case pattern can be calculated using:

$$I_I = C_T V_I 0.5 f_C \times 21 \text{ (data outputs)} + C_T V_I f_C \times 1 \text{ (clock output)}$$

where:

I_I = incremental supply current
C_T = total internal (C_{INT}) and external (C_L) load capacitance
V_I = incremental supply voltage
f_C = output clock switching frequency

The incremental current is added to (for V_{CCO} > 3.6V) or subtracted from (for V_{CCO} < 3.6V) the *DC Electrical Characteristics* table maximum supply current. The internal output buffer capacitance is C_{INT} = 6pF. The worst-case pattern switching frequency of the data outputs is half the switching frequency of the output clock.

In the following example, the incremental supply current is calculated for V_{CCO} = 5.5V, f_C = 34MHz, and C_L = 8pF:

$$V_I = 5.5V - 3.6V = 1.9V$$

$$C_T = C_{INT} + C_L = 6pF + 8pF = 14pF$$

where:

$I_I = C_T V_I 0.5 F_C \times 21$ (data outputs) + $C_T V_I f_C \times 1$ (clock output)

I_I = (14pF x 1.9V x 0.5 x 34MHz x 21) + (14pF x 1.9V x 34MHz)

I_I = 9.5mA + 0.9mA = 10.4mA

The maximum supply current in DC-balanced mode for V_{CC} = V_{CCO} = 3.6V at f_C = 34MHz is 106mA (from the *DC Electrical Characteristics* table). Add 10.4mA to get the total approximate maximum supply current at V_{CCO} = 5.5V and V_{CC} = 3.6V.

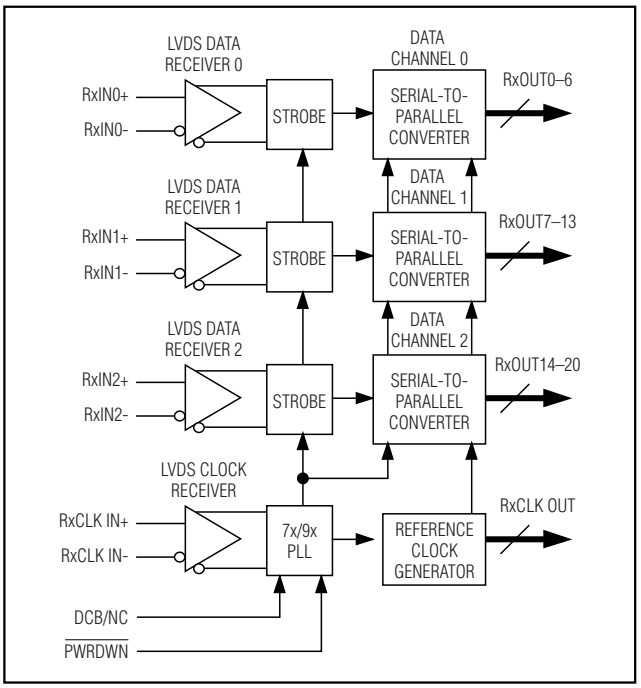
If the output supply voltage is less than V_{CCO} = 3.6V, the reduced supply current can be calculated using the same formula and method.

At high switching frequency, high supply voltage, and high capacitive loading, power dissipation can exceed the package power dissipation rating. Do not exceed the maximum package power dissipation rating. See the *Absolute Maximum Ratings* for maximum package power dissipation capacity and temperature derating.

Rising- or Falling-Edge Output Strobe

The MAX9210/MAX9212/MAX9214/MAX9216 have a rising-edge output strobe, which latches the parallel output data into the next chip on the rising edge of RxCLK OUT. The MAX9220/MAX9222 have a falling-edge output strobe, which latches the parallel output data into the next chip on the falling edge of RxCLK OUT. The deserializer output strobe polarity does not need to match the serializer input strobe polarity. A deserializer with rising or falling edge output strobe can be driven by a serializer with a rising edge input strobe.

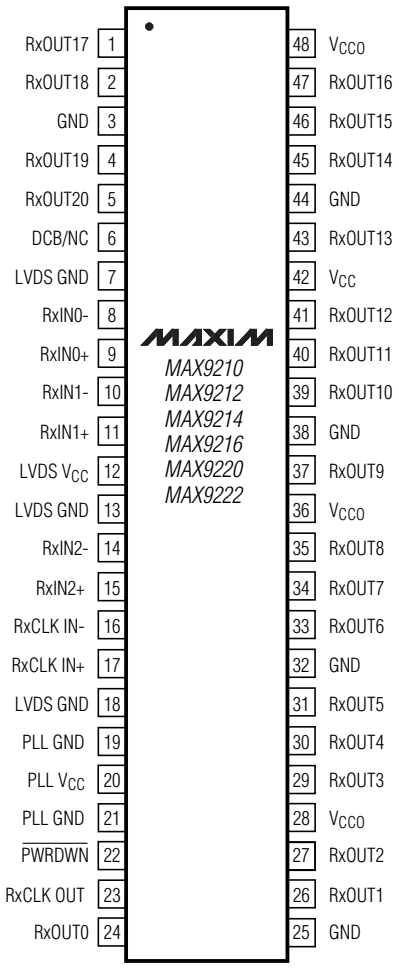
Functional Diagram



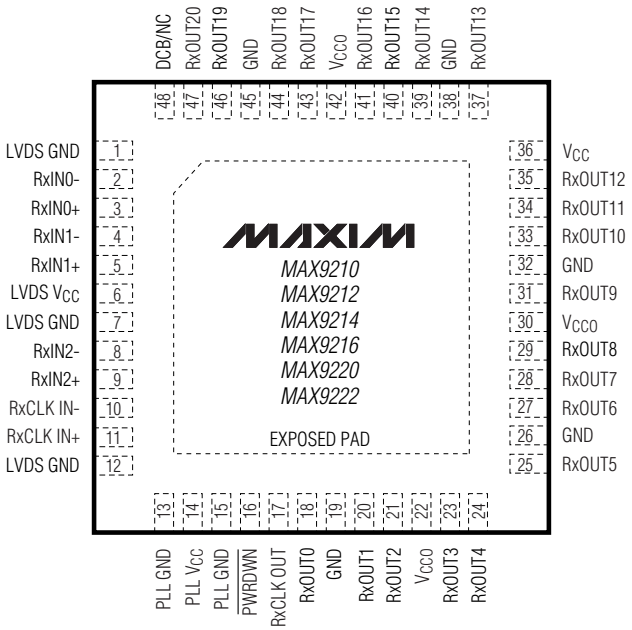
Programmable DC-Balance 21-Bit Deserializers

Pin Configurations

TOP VIEW



TSSOP



QFN

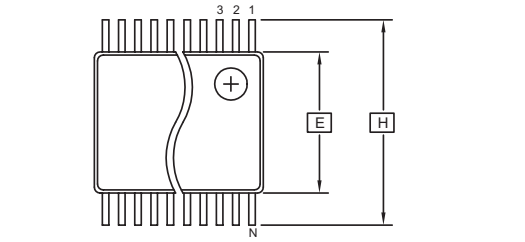
Chip Information

MAX9210 TRANSISTOR COUNT: 10,248
MAX9212 TRANSISTOR COUNT: 10,248
MAX9214 TRANSISTOR COUNT: 10,248
MAX9216 TRANSISTOR COUNT: 10,248
MAX9220 TRANSISTOR COUNT: 10,248
MAX9222 TRANSISTOR COUNT: 10,248
PROCESS: CMOS

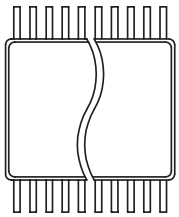
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

48L TSSOP.EPS

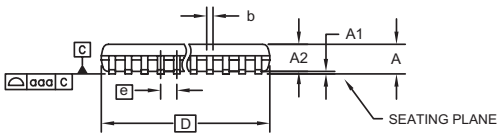


TOP VIEW

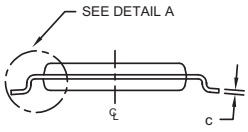


BOTTOM VIEW

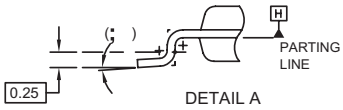
SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	--	--	1.10
A1	0.05	--	0.15
A2	0.55	0.90	0.95
aaa		0.10	
b	0.17	--	0.27
b1	0.17	0.20	0.23
bbb		0.08	
c	0.09	--	0.20
c1	0.09	0.127	0.16
D	12.40	12.50	12.60
E	6.00	6.10	6.20
e		0.50 BSC	
H		8.10 BSC	
L	0.50	0.60	0.75
N		48	
∠	0°	--	8°



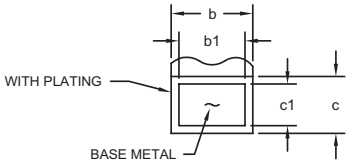
SIDE VIEW



END VIEW



DETAIL A



SECTION C-C

NOTES:

1. DIMENSIONS D & E ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM ON D SIDE, AND 0.25MM ON E SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153, VARIATIONS, ED.
5. "N" REFERS TO NUMBER OF LEADS.
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM (-C-), THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM (-C-) IN THE DIRECTION INDICATED.

MAXIM

PROPRIETARY INFORMATION

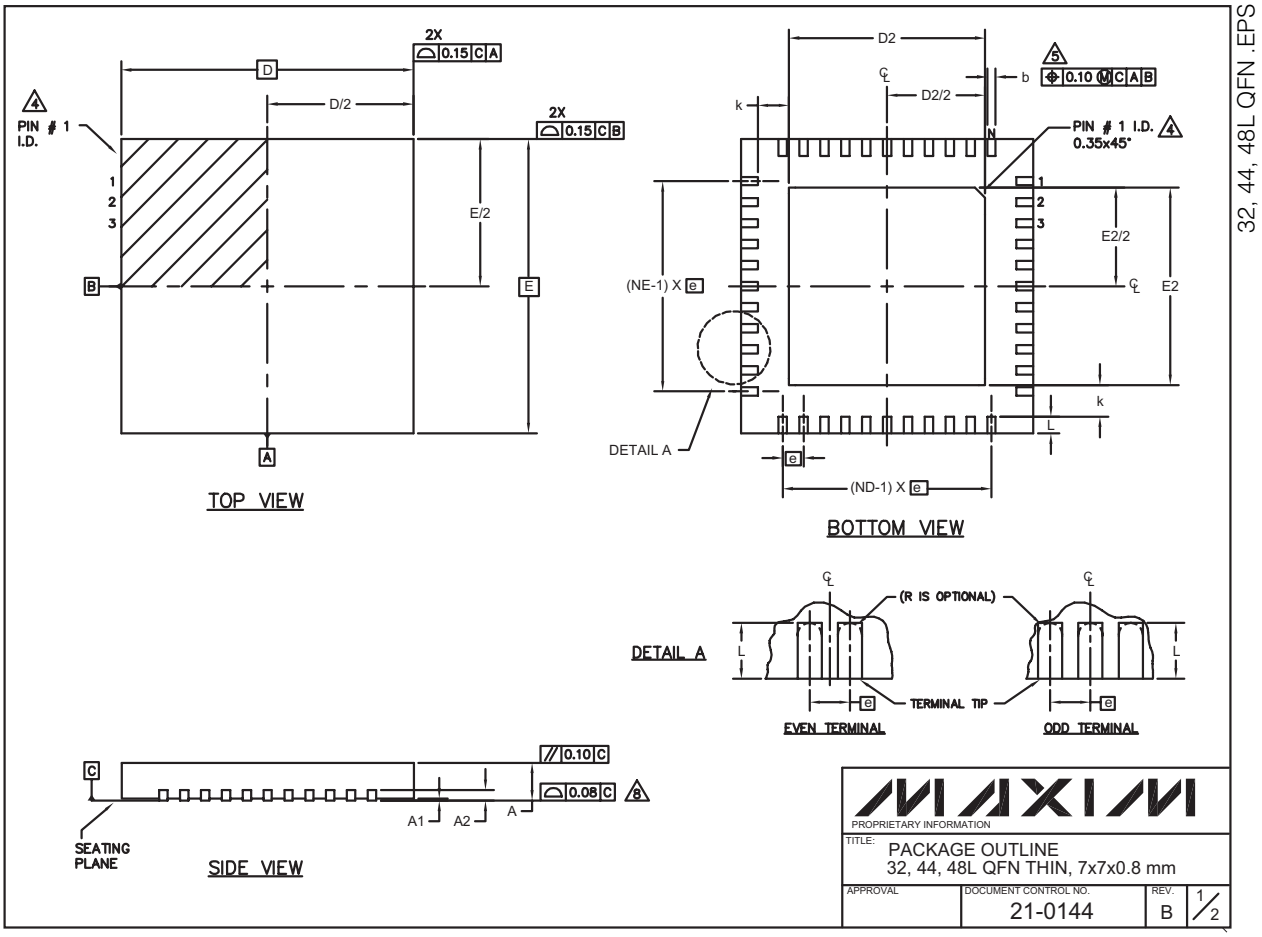
TITLE: PACKAGE OUTLINE, 48L TSSOP, 6.1mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0155	A	1/2

Programmable DC-Balance 21-Bit Deserializers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS								
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.63	5.45	5.60	5.63	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48L QFN THIN, 7x7x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	B	2/2