



8-Port I/O Expander with LED Intensity Control and Interrupt

MAX7315

General Description

The MAX7315 I²C™-/SMBus-compatible serial interfaced peripheral provides microprocessors with 8 I/O ports. Each I/O port can be individually configured as either an open-drain current-sinking output rated at 50mA at 5.5V, or a logic input with transition detection. A ninth port can be used for transition detection interrupt or as a general-purpose output. The outputs are capable of directly driving LEDs, or providing logic outputs with external resistive pullup up to 5.5V.

PWM current drive is integrated with 8 bits of control. Four bits are global control and apply to all LED outputs to provide coarse adjustment of current from fully off to fully on in 14 intensity steps. Each output then has individual 4-bit control, which further divides the globally set current into 16 more steps. Alternatively, the current control can be configured as a single 8-bit control that sets all outputs at once.

The MAX7315 is pin and software compatible with the PCA9534 and PCA9554(A).

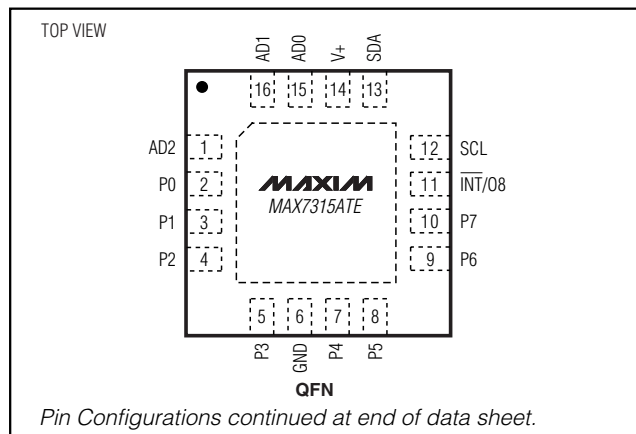
Each output has independent blink timing with two blink phases. All LEDs can be individually set to be on or off during either blink phase, or to ignore the blink control. The blink period is controlled by a register.

The MAX7315 is controlled through the 2-wire I²C/SMBus serial interface, and can be configured to one of 64 I²C addresses.

Applications

- LCD Backlights
- LED Status Indication
- Portable Equipment
- Laptop Computers
- Keypad Backlights
- RGB LED Drivers
- Cellular Phones

Pin Configurations



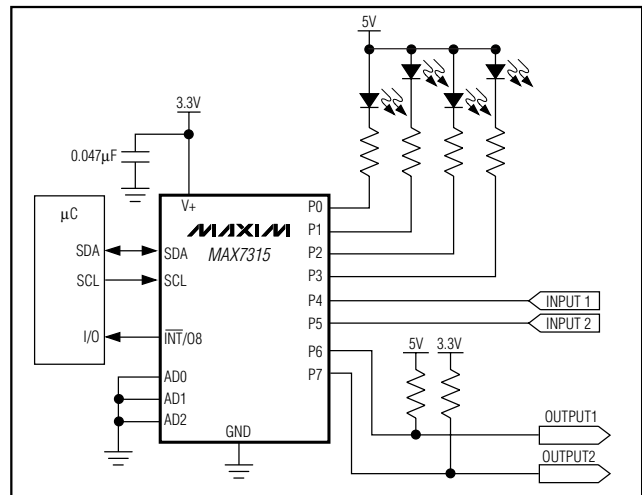
Features

- ◆ 400kbps, 2-Wire Serial Interface, 5.5V Tolerant
- ◆ 2V to 3.6V Operation
- ◆ Overall 8-Bit PWM LED Intensity Control
Global 16-Step Intensity Control
Plus Individual 16-Step Intensity Control
- ◆ Automatic Two-Phase LED Blinking
- ◆ 50mA Maximum Port Output Current
- ◆ Outputs Are 5.5V-Rated Open Drain
- ◆ Inputs Are Overvoltage Protected to 5.5V
- ◆ Transition Detection with Interrupt Output
- ◆ Low Standby Current (1.2µA typ; 3.3µA max)
- ◆ Tiny 3mm x 3mm, Thin QFN Package
- ◆ -40°C to +125°C Temperature Range
- ◆ All Ports Can Be Configured as Inputs or Outputs

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|------------|-----------------|-------------------------------------|----------|
| MAX7315ATE | -40°C to +125°C | 16 Thin QFN 3mm x 3mm x 0.8mm | AAU |
| MAX7315AEE | -40°C to +125°C | 16 QSOP | — |
| MAX7315AUE | -40°C to +125°C | 16 TSSOP | — |

Typical Application Circuit



Purchase of I²C components of Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.



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ABSOLUTE MAXIMUM RATINGS

| | | |
|---|--------------|--|
| Voltage (with respect to GND) | | 16-Pin TSSOP (derate 9.4mW/°C over +70°C)754mW |
| V+ | -0.3V to +4V | 16-Pin QSOP (derate 8.3mW/°C over +70°C).....666mW |
| SCL, SDA, AD0, AD1, AD2, P0–P7 | -0.3V to +6V | 16-Pin QFN (derate 14.7mW/°C over +70°C)1176mW |
| INT/O8 | -0.3V to +8V | Operating Temperature Range (T _{MIN} to T _{MAX})-40°C to +125°C |
| DC Current on P0–P7, INT/O8 | 55mA | Junction Temperature |
| DC Current on SDA | 10mA | Storage Temperature Range |
| Maximum GND Current | 190mA | Lead Temperature (soldering, 10s) |
| Continuous Power Dissipation (T _A = +70°C) | | |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, V+ = 2V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------------------|--|---|----------|------|-------|
| Operating Supply Voltage | V+ | | 2 | | 3.6 | V |
| Output Load External Supply Voltage | V _{EXT} | | 0 | | 5.5 | V |
| Standby Current (Interface Idle, PWM Disabled) | I ₊ | SCL and SDA at V+; other digital inputs at V+ or GND; PWM intensity control disabled | T _A = +25°C | 1.2 | 2.3 | μA |
| | | | T _A = -40°C to +85°C | | 2.6 | |
| | | | T _A = T _{MIN} to T _{MAX} | | 3.3 | |
| Supply Current (Interface Idle, PWM Enabled) | I ₊ | SCL and SDA at V+; other digital inputs at V+ or GND; PWM intensity control enabled | T _A = +25°C | 7 | 12.1 | μA |
| | | | T _A = -40°C to +85°C | | 13.5 | |
| | | | T _A = T _{MIN} to T _{MAX} | | 14.4 | |
| Supply Current (Interface Running, PWM Disabled) | I ₊ | f _{SCL} = 400kHz; other digital inputs at V+ or GND; PWM intensity control disabled | T _A = +25°C | 40 | 76 | μA |
| | | | T _A = -40°C to +85°C | | 78 | |
| | | | T _A = T _{MIN} to T _{MAX} | | 80 | |
| Supply Current (Interface Running, PWM Enabled) | I ₊ | f _{SCL} = 400kHz; other digital inputs at V+ or GND; PWM intensity control enabled | T _A = +25°C | 51 | 110 | μA |
| | | | T _A = -40°C to +85°C | | 117 | |
| | | | T _A = T _{MIN} to T _{MAX} | | 122 | |
| Input High Voltage SDA, SCL, AD0, AD1, AD2, P0–P7 | V _{IH} | | 0.7 × V+ | | | V |
| Input Low Voltage SDA, SCL, AD0, AD1, AD2, P0–P7 | V _{IL} | | | 0.3 × V+ | | V |
| Input Leakage Current SDA, SCL, AD0, AD1, AD2, P0–P7 | I _{IH} , I _{IL} | 0 ≤ input voltage ≤ 5.5V | -0.2 | | +0.2 | μA |
| Input Capacitance SDA, SCL, AD0, AD1, AD2, P0–P7 | | | | 8 | | pF |

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ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit, $V_+ = 2V$ to $3.6V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_+ = 3.3V$, $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------|----------------------------------|--------------------------------------|------|------|-------|
| Output Low Voltage P0–P7, INT/O8 | VOL | $V_+ = 2V$, $I_{SINK} = 20mA$ | $T_A = +25^\circ C$ | 0.15 | 0.25 | V |
| | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | 0.29 | |
| | | | $T_A = T_{MIN}$ to T_{MAX} | | 0.31 | |
| | | $V_+ = 2.5V$, $I_{SINK} = 20mA$ | $T_A = +25^\circ C$ | 0.13 | 0.22 | |
| | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | 0.25 | |
| | | | $T_A = T_{MIN}$ to T_{MAX} | | 0.27 | |
| | | $V_+ = 3.3V$, $I_{SINK} = 20mA$ | $T_A = +25^\circ C$ | 0.12 | 0.22 | |
| | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | 0.23 | |
| | | | $T_A = T_{MIN}$ to T_{MAX} | | 0.25 | |
| Output Low-Voltage SDA | VOLSDA | $I_{SINK} = 6mA$ | | | 0.4 | V |
| PWM Clock Frequency | f _{PWM} | | | 32 | | kHz |

TIMING CHARACTERISTICS

(Typical Operating Circuit, $V_+ = 2V$ to $3.6V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_+ = 3.3V$, $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------------------|--------------|-----|----------------------------|-----|-------|
| Serial Clock Frequency | f _{SCL} | | | | 400 | kHz |
| Bus Free Time Between a STOP and a START Condition | t _{BUF} | | 1.3 | | | μs |
| Hold Time, Repeated START Condition | t _{HD, STA} | | 0.6 | | | μs |
| Repeated START Condition Setup Time | t _{SU, STA} | | 0.6 | | | μs |
| STOP Condition Setup Time | t _{SU, STO} | | 0.6 | | | μs |
| Data Hold Time | t _{HD, DAT} | (Note 2) | | | 0.9 | μs |
| Data Setup Time | t _{SU, DAT} | | 180 | | | ns |
| SCL Clock Low Period | t _{LOW} | | 1.3 | | | μs |
| SCL Clock High Period | t _{HIGH} | | 0.7 | | | μs |
| Rise Time of Both SDA and SCL Signals, Receiving | t _R | (Notes 3, 4) | | 200 + 0.1C _b | 300 | ns |
| Fall Time of Both SDA and SCL Signals, Receiving | t _F | (Notes 3, 4) | | 200 + 0.1C _b | 300 | ns |
| Fall Time of SDA Transmitting | t _{F, TX} | (Notes 3, 5) | | 200 + 0.1C _b | 250 | ns |
| Pulse Width of Spike Suppressed | t _{SP} | (Note 6) | | 50 | | ns |
| Capacitive Load for Each Bus Line | C _b | (Note 3) | | | 400 | pF |

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TIMING CHARACTERISTICS (continued)

(Typical Operating Circuit, $V_+ = 2V$ to $3.6V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_+ = 3.3V$, $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|----------|------------|-----|-----|-----|---------|
| Interrupt Valid | t_{IV} | Figure 10 | | | 6.5 | μs |
| Interrupt Reset | t_{IR} | Figure 10 | | | 1 | μs |
| Output Data Valid | t_{DV} | Figure 10 | | | 5 | μs |
| Input Data Step Time | t_{DS} | Figure 10 | 100 | | | ns |
| Input Data Hold Time | t_{DH} | Figure 10 | 1 | | | μs |

Note 1: All parameters tested at $T_A = +25^\circ C$. Specifications over temperature are guaranteed by design.

Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 3: Guaranteed by design.

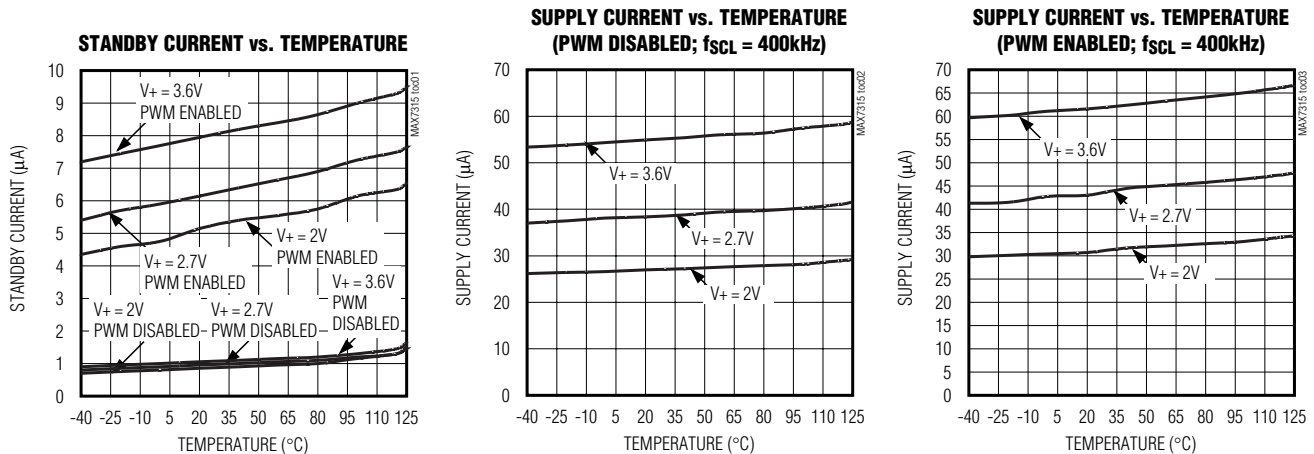
Note 4: C_b = total capacitance of one bus line in pF. t_r and t_f measured between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

Note 5: $I_{SINK} \leq 6mA$. C_b = total capacitance of one bus line in pF. t_r and t_f measured between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)



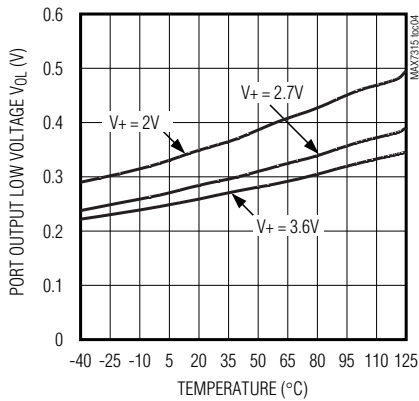
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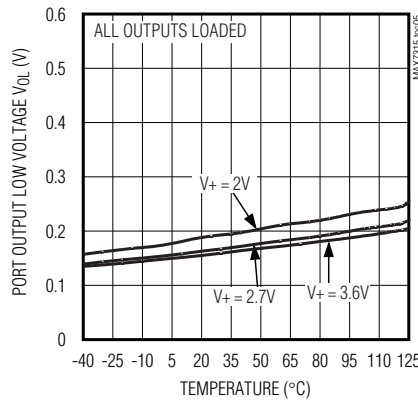
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

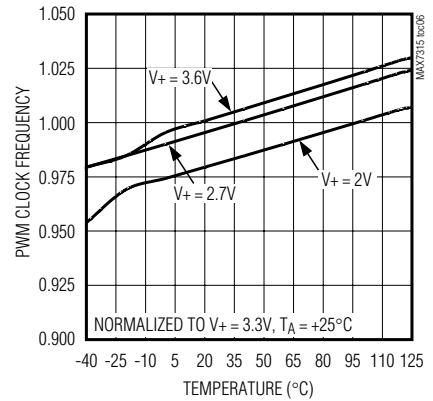
PORT OUTPUT LOW VOLTAGE WITH 50mA LOAD CURRENT vs. TEMPERATURE



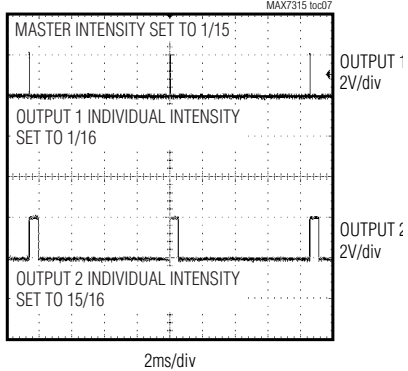
PORT OUTPUT LOW VOLTAGE WITH 20mA LOAD CURRENT vs. TEMPERATURE



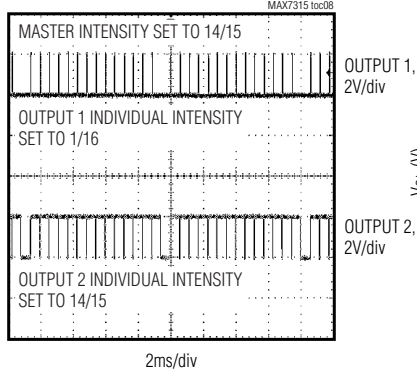
PWM CLOCK FREQUENCY vs. TEMPERATURE



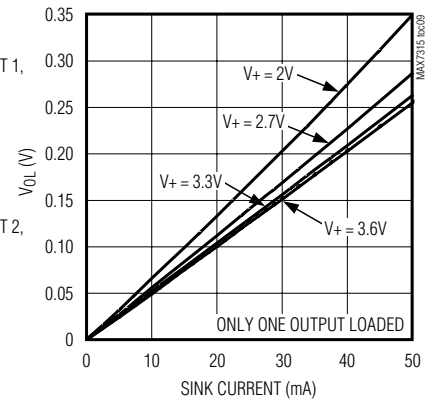
SCOPE SHOT OF 2 OUTPUT PORTS



SCOPE SHOT OF 2 OUTPUT PORTS



SINK CURRENT vs. V_OL



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Pin Description

| PIN | | NAME | FUNCTION |
|------------|-----------|-----------------------------------|---|
| QSOP/TSSOP | QFN | | |
| 1, 2, 3 | 15, 16, 1 | AD0, AD1, AD2 | Address Inputs. Sets device slave address. Connect to either GND, V+, SCL, or SDA to give 64 logic combinations. See Table 1. |
| 4–7, 9–12 | 2–5, 7–10 | P0–P7 | Input/Output Ports. P0–P7 are open-drain I/Os rated at 5.5V, 50mA. |
| 8 | 6 | GND | Ground. Do not sink more than 190mA into the GND pin. |
| 13 | 11 | $\overline{\text{INT}}/\text{O8}$ | Output Port. Open-drain output rated at 7.0V, 50mA. Configurable as interrupt output or general-purpose output. |
| 14 | 12 | SCL | I ² C-Compatible Serial Clock Input |
| 15 | 13 | SDA | I ² C-Compatible Serial Data I/O |
| 16 | 14 | V+ | Positive Supply Voltage. Bypass V+ to GND with a 0.047 μ F ceramic capacitor |
| — | PAD | Exposed pad | Exposed Pad on Package Underside. Connect to GND. |

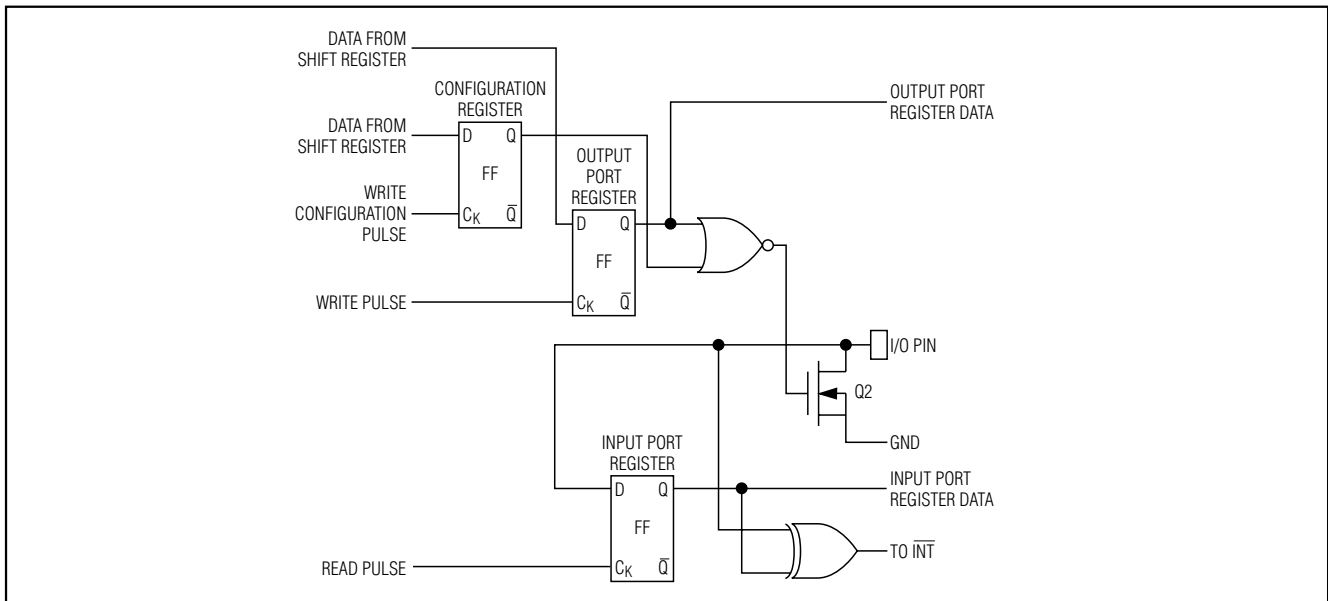


Figure 1. Simplified Schematic of I/O Ports

Functional Overview

The MAX7315 is a general-purpose input/output (GPIO) peripheral that provides eight I/O ports, P0–P7, controlled through an I²C-compatible serial interface. A 9th output-only port, $\overline{\text{INT}}/\text{O8}$, can be configured as an interrupt output or as a general-purpose output port. All output ports sink loads up to 50mA connected to external supplies up to 5.5V, independent of the MAX7315's

supply voltage. The MAX7315 is rated for a ground current of 190mA, allowing all nine outputs to sink 20mA at the same time. Figure 1 shows the output structure of the MAX7315. The ports default to inputs on power-up.

Port Inputs and Transition Detection

An input ports register reflects the incoming logic levels of the port pins, regardless of whether the pin is defined as an input or an output. Reading the input

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ports register latches the current-input logic level of the affected eight ports. Transition detection allows all ports configured as inputs to be monitored for changes in their logic status. The action of reading the input ports register samples the corresponding 8 port bits' input condition. This sample is continuously compared with the actual input conditions. A detected change in input condition causes the $\overline{\text{INT}}/\text{O8}$ interrupt output to go low, if configured as an interrupt output. The interrupt is cleared either automatically if the changed input returns to its original state, or when the input ports register is read.

The $\overline{\text{INT}}/\text{O8}$ pin can be configured as either an interrupt output or as a 9th output port with the same static or blink controls as the other eight ports (Table 4).

Port Output Control and LED Blinking

The blink phase 0 register sets the output logic levels of the eight ports P0–P7 (Table 8). This register controls the port outputs if the blink function is disabled. A duplicate register, the blink phase 1 register, is also used if the blink function is enabled (Table 9). In blink mode, the port outputs can be flipped between using the blink phase 0 register and the blink phase 1 register using software control (the blink flip flag in the configuration register) (Table 4).

PWM Intensity Control

The MAX7315 includes an internal oscillator, nominally 32kHz, to generate PWM timing for LED intensity control. PWM intensity control can be enabled on an output-by-output basis, allowing the MAX7315 to provide any mix of PWM LED drives and glitch-free logic outputs (Table 10). PWM can be disabled entirely, in which case all output ports are static and the MAX7315 operating current is lowest because the internal oscillator is turned off.

PWM intensity control uses a 4-bit master control and 4 bits of individual control per output (Tables 13, 14). The 4-bit master control provides 16 levels of overall intensity control, which applies to all PWM-enabled output ports. The master control sets the maximum pulse width from 1/15 to 15/15 of the PWM time period. The individual settings comprise a 4-bit number further reducing the duty cycle to be from 1/16 to 15/16 of the time window set by the master control.

For applications requiring the same PWM setting for all output ports, a single global PWM control can be used instead of all the individual controls to simplify the control software and provide 240 steps of intensity control (Tables 10 and 13).

Standby Mode

When the serial interface is idle and the PWM intensity control is unused, the MAX7315 automatically enters standby mode. If the PWM intensity control is used, the operating current is slightly higher because the internal PWM oscillator is running. When the serial interface is active, the operating current also increases because the MAX7315, like all I²C slaves, has to monitor every transmission.

Serial Interface

Serial Addressing

The MAX7315 operates as a slave that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX7315 and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX7315 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7k Ω , is required on SDA. The MAX7315 SCL line operates

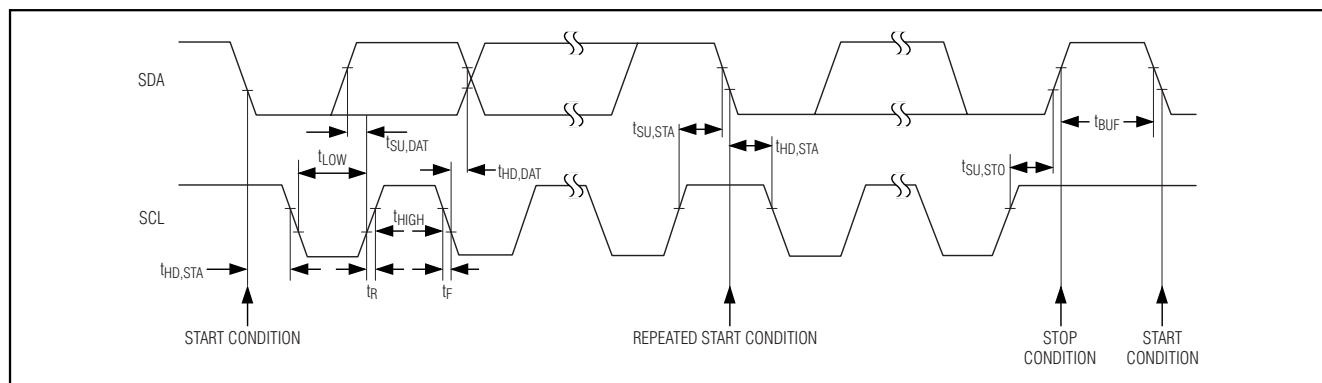


Figure 2. 2-Wire Serial Interface Timing Details

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only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX7315 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA

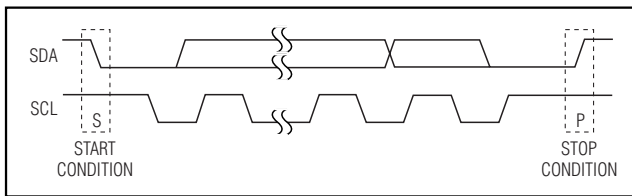


Figure 3. Start and Stop Conditions

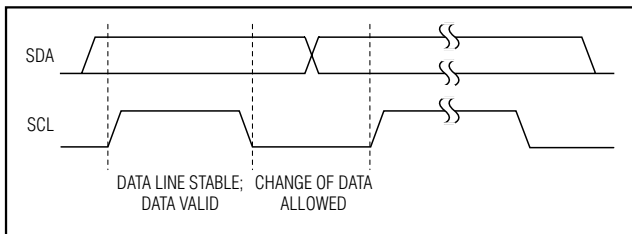


Figure 4. Bit Transfer

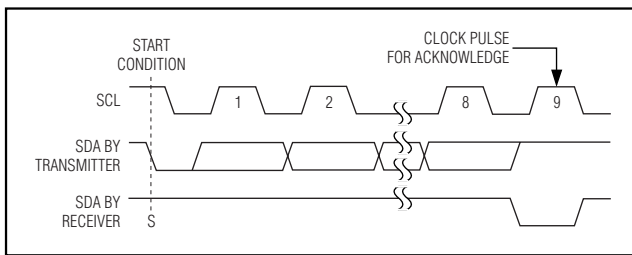


Figure 5. Acknowledge

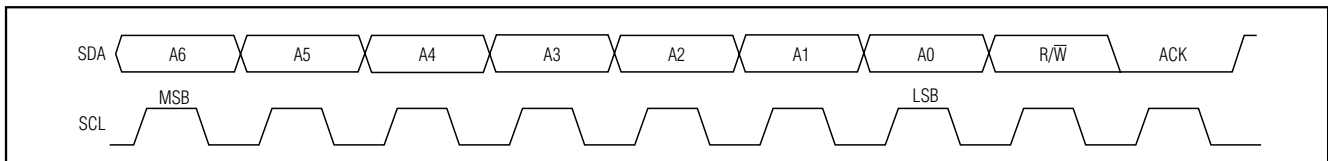


Figure 6. Slave Address

from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7315, the device generates the acknowledge bit because the MAX7315 is the recipient. When the MAX7315 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7315 has a 7-bit long slave address (Figure 6). The eighth bit following the 7-bit slave address is the R/W bit. The R/W bit is low for a write command, high for a read command.

The slave address bits A6 through A0 are selected by the address inputs AD0, AD1, and AD2. These pins can be connected to GND, V+, SDA, or SCL. The MAX7315 has 64 possible slave addresses (Table 1) and, therefore, a maximum of 64 MAX7315 devices can be controlled independently from the same interface.

Message Format for Writing the MAX7315

A write to the MAX7315 comprises the transmission of the MAX7315's slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX7315 is to be written to by the next byte, if received (Table 2). If a STOP condition is detected after the command byte is received, then the MAX7315 takes no further action beyond storing the command byte.

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Table 1. MAX7315 I²C Slave Address Map

| PIN AD2 | PIN AD1 | PIN AD0 | DEVICE ADDRESS | | | | | | |
|---------|---------|---------|----------------|----|----|----|----|----|----|
| | | | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| GND | SCL | GND | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| GND | SCL | V+ | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| GND | SDA | GND | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| GND | SDA | V+ | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| V+ | SCL | GND | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| V+ | SCL | V+ | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| V+ | SDA | GND | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| V+ | SDA | V+ | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| GND | SCL | SCL | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GND | SCL | SDA | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| GND | SDA | SCL | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| GND | SDA | SDA | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| V+ | SCL | SCL | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| V+ | SCL | SDA | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| V+ | SDA | SCL | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| V+ | SDA | SDA | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| GND | GND | GND | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| GND | GND | V+ | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| GND | V+ | GND | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| GND | V+ | V+ | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| V+ | GND | GND | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| V+ | GND | V+ | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| V+ | V+ | GND | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| V+ | V+ | V+ | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| GND | GND | SCL | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| GND | GND | SDA | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| GND | V+ | SCL | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| GND | V+ | SDA | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| V+ | GND | SCL | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| V+ | GND | SDA | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| V+ | V+ | SCL | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| V+ | V+ | SDA | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

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Table 1. MAX7315 I²C Slave Address Map (continued)

| PIN AD2 | PIN AD1 | PIN AD0 | DEVICE ADDRESS | | | | | | |
|---------|---------|---------|----------------|----|----|----|----|----|----|
| | | | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| SCL | SCL | GND | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| SCL | SCL | V+ | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| SCL | SDA | GND | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| SCL | SDA | V+ | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| SDA | SCL | GND | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| SDA | SCL | V+ | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| SDA | SDA | GND | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| SDA | SDA | V+ | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| | | | | | | | | | |
| SCL | SCL | SCL | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| SCL | SCL | SDA | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| SCL | SDA | SCL | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| SCL | SDA | SDA | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| SDA | SCL | SCL | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| SDA | SCL | SDA | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| SDA | SDA | SCL | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| SDA | SDA | SDA | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | | | | | | | | |
| SCL | GND | GND | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| SCL | GND | V+ | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| SCL | V+ | GND | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| SCL | V+ | V+ | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| SDA | GND | GND | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| SDA | GND | V+ | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| SDA | V+ | GND | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| SDA | V+ | V+ | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| | | | | | | | | | |
| SCL | GND | SCL | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| SCL | GND | SDA | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| SCL | V+ | SCL | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| SCL | V+ | SDA | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| SDA | GND | SCL | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| SDA | GND | SDA | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| SDA | V+ | SCL | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| SDA | V+ | SDA | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

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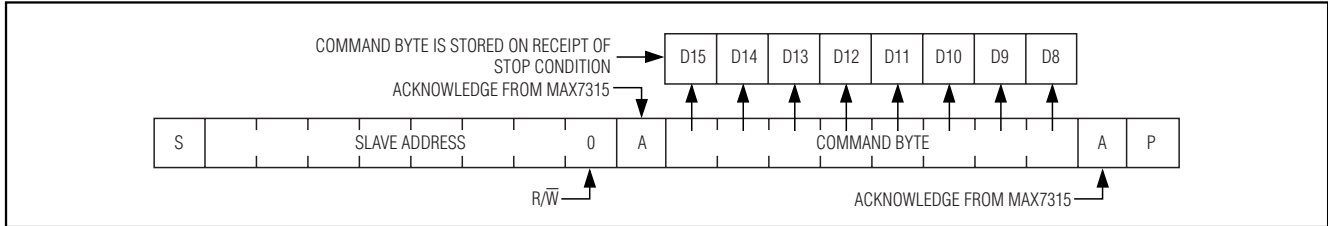


Figure 7. Command Byte Received

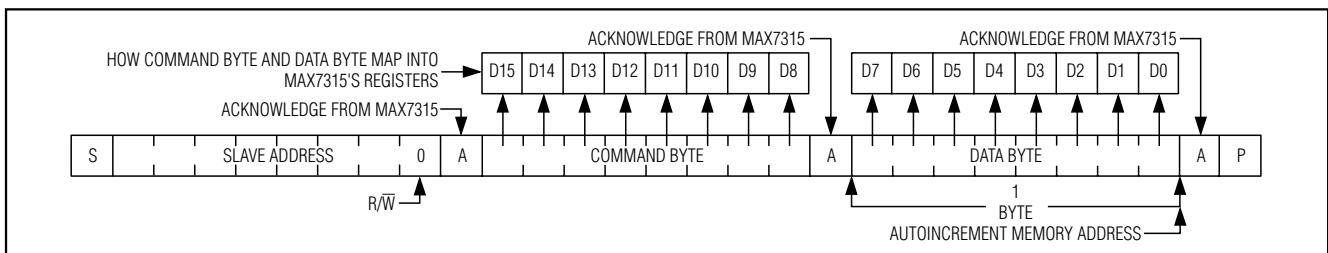


Figure 8. Command and Single Data Byte Received

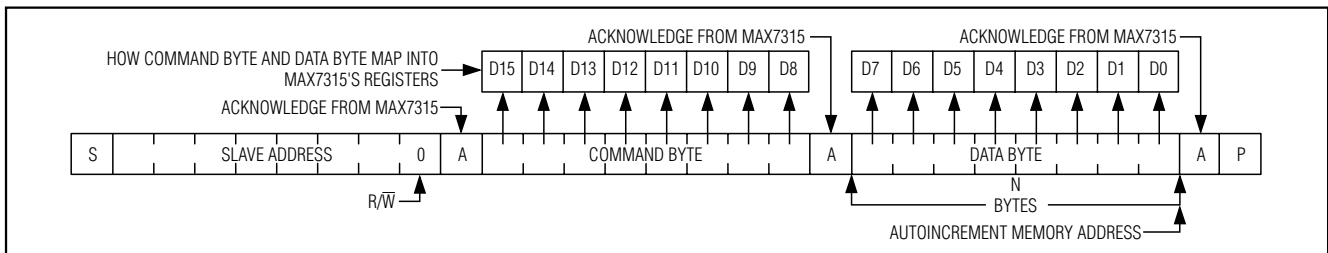


Figure 9. n Data Bytes Received

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX7315 selected by the command byte (Figure 8). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX7315 internal registers because the command byte address autoincrements (Table 2). A diagram of a write to the output ports registers (blink phase 0 register or blink phase 1 register) is given in Figure 10.

Message Format for Reading

The MAX7315 is read using the MAX7315's internally stored command byte as an address pointer the same way the stored command byte is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write (Table 2). Thus, a read is initiated by first configuring the MAX7315's command byte by performing a write (Figure 7). The master can now read n consecu-

tive bytes from the MAX7315 with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address has been autoincremented after the write (Table 2). A diagram of a read from the input ports register is shown in Figure 10 reflecting the states of the ports.

Operation with Multiple Masters

If the MAX7315 is operated on a 2-wire interface with multiple masters, a master reading the MAX7315 should use a repeated start between the write, which sets the MAX7315's address pointer, and the read(s) that takes the data from the location(s) (Table 2). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX7315's address pointer but before master 1 has read the data. If master 2 subsequently changes the MAX7315's address pointer, then master 1's delayed read can be from an unexpected location.

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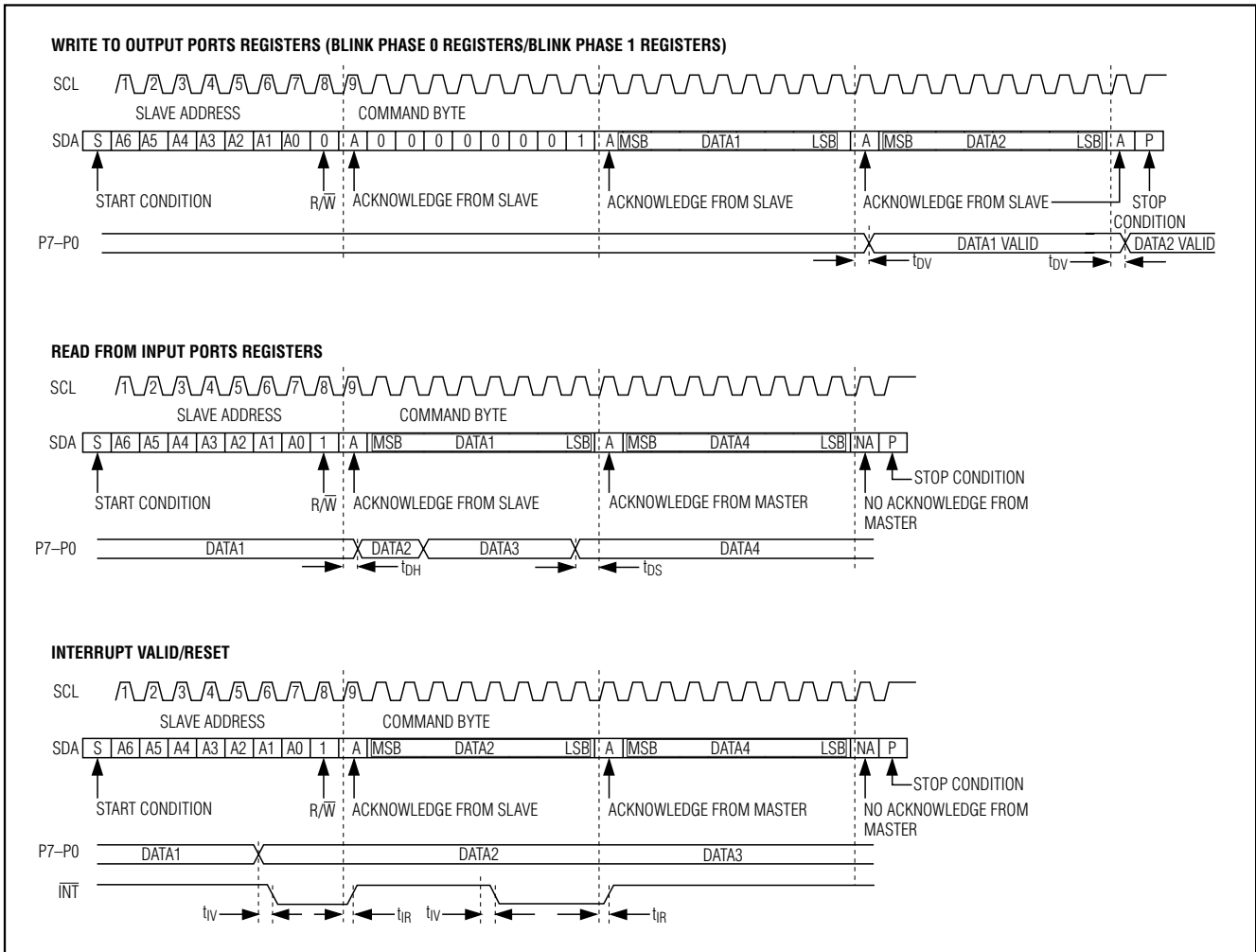


Figure 10. Read, Write, and Interrupt Timing Diagrams

Command Address Autoincrementing

The command address stored in the MAX7315 circulates around grouped register functions after each data byte is written or read (Table 2).

Device Reset

If a device reset input is needed, consider the MAX7316. The MAX7316 includes a $\overline{\text{RST}}$ input, which clears any transaction to or from the MAX7316 on the serial interface and configures the internal registers to the same state as a power-up reset.

Detailed Description

Initial Power-Up

On power-up all control registers are reset and the MAX7315 enters standby mode (Table 3). Power-up status makes all ports into inputs and disables both the PWM oscillator and blink functionality.

Configuration Register

The configuration register is used to configure the PWM intensity mode, interrupt, and blink behavior, operate the $\overline{\text{INT/O8}}$ output, and read back the interrupt status (Table 4).

8-Port I/O Expander with LED Intensity Control and Interrupt

Table 2. Register Address Map

| REGISTER | ADDRESS CODE (HEX) | AUTOINCREMENT ADDRESS |
|--------------------------|--------------------|-----------------------|
| Read input ports | 0x00 | 0x00 (no change) |
| Blink phase 0 outputs | 0x01 | 0x01 (no change) |
| Ports configuration | 0x03 | 0x03 (no change) |
| Blink phase 1 outputs | 0x09 | 0x09 (no change) |
| Master, O8 intensity | 0x0E | 0x0E (no change) |
| Configuration | 0x0F | 0x0F (no change) |
| Outputs intensity P1, P0 | 0x10 | 0x11 |
| Outputs intensity P3, P2 | 0x11 | 0x12 |
| Outputs intensity P5, P4 | 0x12 | 0x13 |
| Outputs intensity P7, P6 | 0x13 | 0x10 |

Ports Configuration

The 8 I/O ports P0 through P7 can be configured to any combination of inputs and outputs using the ports configuration register (Table 5). The $\overline{\text{INT/O8}}$ output can also be configured as an extra general-purpose output using the configuration register (Table 4).

Input Ports

The input ports register is read only (Table 6). It reflect the incoming logic levels of the ports, regardless of whether the port is defined as an input or an output by the ports configuration register. Reading the input ports register latches the current-input logic level of the affected eight ports. A write to the input ports register is ignored.

Transition Detection

All ports configured as inputs are always monitored for changes in their logic status. The action of reading the input ports register or writing to the configuration register samples the corresponding 8 port bits' input condition (Tables 4, 6). This sample is continuously compared with the actual input conditions. A detected change in input condition causes an interrupt condition. The interrupt is cleared either automatically if the changed input returns to its original state, or when the input ports register is read, updating the compared data (Figure 10). Randomly changing a port from an output to an input may cause a false interrupt to occur if the state of the input does not match the content of the input ports register. The interrupt status is available as the interrupt flag $\overline{\text{INT}}$ in the configuration register (Table 4).

The input status of all ports is sampled immediately after power-up as part of the MAX7315's internal initial-

ization, so if all the ports are pulled to valid logic levels at that time an interrupt does not occur at power-up.

$\overline{\text{INT/O8}}$ Output

The $\overline{\text{INT/O8}}$ output pin can be configured as either the $\overline{\text{INT}}$ output that reflects the interrupt flag logic state or as a general-purpose output O8. When used as a general-purpose output, the $\overline{\text{INT/O8}}$ pin has the same blink and PWM intensity control capabilities as the other ports.

Set the interrupt enable I bit in the configuration register to configure $\overline{\text{INT/O8}}$ as the $\overline{\text{INT}}$ output (Table 4). Clear interrupt enable to configure $\overline{\text{INT/O8}}$ as the O8. O8 logic state is set by the 2 bits O1 and O0 in the configuration register. O8 follows the rules for blinking selected by the blink enable flag E in the configuration register. If blinking is disabled, then interrupt output control O0 alone sets the logic state of the $\overline{\text{INT/O8}}$ pin. If blinking is enabled, then both interrupt output controls O0 and O1 set the logic state of the $\overline{\text{INT/O8}}$ pin according to the blink phase. PWM intensity control for O8 is set by the 4 global intensity bits in the master, O8 intensity register (Table 13).

Blink Mode

In blink mode, the output ports can be flipped between using either the blink phase 0 register or the blink phase 1 register. Flip control is by software control (the blink flip flag B in the configuration register) (Table 4). If hardware flip control is needed, consider the MAX7316, which includes a BLINK input, as well as software control.

The blink function can be used for LED effects by programming different display patterns in the two sets of

8-Port I/O Expander with LED Intensity Control and Interrupt

Table 3. Power-Up Configuration

| REGISTER FUNCTION | POWER-UP CONDITION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|-----------------------------|---|--------------------|---------------|----|----|----|----|----|----|----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Blink phase 0 outputs P7–P0 | High-impedance outputs | 0x01 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ports configuration P7–P0 | Ports P7–P0 are inputs | 0x03 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Blink phase 1 outputs P7–P0 | High-impedance outputs | 0x09 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Master, O8 intensity | PWM oscillator is disabled; O8 is static logic output | 0x0E | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Configuration | $\overline{\text{INT}}$ /O8 is interrupt output; blink is disabled; global intensity is enabled | 0x0F | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Outputs intensity P1, P0 | P1, P0 are static logic outputs | 0x10 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Outputs Intensity P3, P2 | P3, P2 are static logic outputs | 0x11 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Outputs intensity P5, P4 | P5, P4 are static logic outputs | 0x12 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Outputs intensity P7, P6 | P7, P6 are static logic outputs | 0x13 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 4. Configuration Register

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|---|-----|--------------------|-------------------------|----|---------------------------------|------------------|------------------|------------|--------------|----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CONFIGURATION | | | INTERRUPT STATUS | — | INTERRUPT OUTPUT CONTROL AS GPO | INTERRUPT ENABLE | GLOBAL INTENSITY | BLINK FLIP | BLINK ENABLE | |
| Write device configuration | 0 | 0x0F | $\overline{\text{INT}}$ | X | O1 | O0 | I | G | B | E |
| Read-back device configuration | 1 | | O | | | | | | | |
| Disable blink | — | | X | X | X | X | X | X | X | 0 |
| Enable blink | — | | X | X | X | X | X | X | X | 1 |
| Flip blink register (see text) | — | | X | X | X | X | X | X | 0 | 1 |
| | — | | X | X | X | X | X | X | 1 | 1 |
| Disable global intensity control—intensity is set by registers 0x10–0x13 for ports P0 through P7 when configured as outputs, and by D3–D7 of register 0x0E for $\overline{\text{INT}}$ /O8 when $\overline{\text{INT}}$ /O8 pin is configured as an output port | — | | X | X | X | X | X | 0 | X | X |
| Enable global intensity control—intensity for all ports configured as outputs is set by D3–D0 of register 0x0E | — | | X | X | X | X | X | 1 | X | X |

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Table 4. Configuration register (continued)

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|--|-----|--------------------|-------------------------|--------|---------------------------------|------------------|------------------|------------|--------------|----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CONFIGURATION | | | INTERRUPT STATUS | — | INTERRUPT OUTPUT CONTROL AS GPO | INTERRUPT ENABLE | GLOBAL INTENSITY | BLINK FLIP | BLINK ENABLE | |
| Disable data change interrupt— $\overline{\text{INT}}/\text{O8}$ output is controlled by the O0 and O1 bits | — | 0x0F | $\overline{\text{INT}}$ | X O | O1 O0 | I | G | B | E | |
| Enable data change interrupt— $\overline{\text{INT}}/\text{O8}$ output is controlled by port input data change | — | | X | X | X | X | 1 | X | X | X |
| $\overline{\text{INT}}/\text{O8}$ output is low (blink is disabled) | — | | X | X | X | 0 | 0 | X | X | 0 |
| $\overline{\text{INT}}/\text{O8}$ output is high impedance (blink is disabled) | — | | X | X | X | 1 | 0 | X | X | 0 |
| $\overline{\text{INT}}/\text{O8}$ output is low during blink phase 0 | — | | X | X | X | 0 | 0 | X | X | 1 |
| $\overline{\text{INT}}/\text{O8}$ output is high impedance during blink phase 0 | — | | X | X | X | 1 | 0 | X | X | 1 |
| $\overline{\text{INT}}/\text{O8}$ output is low during blink phase 1 | — | | X | X | 0 | X | 0 | X | X | 1 |
| $\overline{\text{INT}}/\text{O8}$ output is high impedance during blink phase 1 | — | | X | X | 1 | X | 0 | X | X | 1 |
| Read-back data change interrupt status —data change is not detected, and $\overline{\text{INT}}/\text{O8}$ output is high when interrupt enable (I bit) is set | 1 | | 0 | 0 | X | X | X | X | X | X |
| Read-back data change interrupt status —data change is detected, and $\overline{\text{INT}}/\text{O8}$ output is low when interrupt enable (I bit) is set | 1 | | 1 | 0 | X | X | X | X | X | X |

output port registers, and using the software or hardware controls to flip between the patterns.

If the blink phase 1 register is written with 0xFF, then the BLINK input can be used as a hardware disable to, for example, instantly turn off an LED pattern programmed into the blink phase 0 register. This technique can be further extended by driving the BLINK input with a PWM signal to modulate the LED current to provide fading effects.

The blink mode is enabled by setting the blink enable flag E in the configuration register (Table 4). When blink mode is enabled, the state of the blink flip flag sets the phase, and the output ports are set by either the blink

phase 0 register or the blink phase 1 register (Table 7).

The blink mode is disabled by clearing the blink enable flag E in the configuration register (Table 4). When blink mode is disabled, the blink phase 0 register alone controls the output ports.

Blink Phase Registers

When the blink function is disabled, the blink phase 0 register sets the logic levels of the 8 ports (P0 through P7) when configured as outputs (Table 8). A duplicate register called the blink phase 1 register is also used if the blink function is enabled (Table 9). A logic high sets the appropriate output port high impedance, while a logic low makes the port go low.

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Table 5. Ports Configuration Register

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|--|-----|--------------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Ports configuration (1 = input, 0 = output) | 0 | 0x03 | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| Read-back ports configuration | 1 | | | | | | | | | |

Table 6. Input Ports Register

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|------------------|-----|--------------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Read input ports | 1 | 0x00 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |

Reading a blink phase register reads the value stored in the register, not the actual port condition. The port output itself may or may not be at a valid logic level, depending on the external load connected.

The 9th output, O8, is controlled through 2 bits in the configuration register, which provide the same static or blink control as the other 8 output ports.

PWM Intensity Control

The MAX7315 includes an internal oscillator, nominally 32kHz, to generate PWM timing for LED intensity control or other applications such as PWM trim DACs. PWM can be disabled entirely for all the outputs. In this case, all outputs are static and the MAX7315 operating current is lowest because the internal PWM oscillator is turned off.

The MAX7315 can be configured to provide any combination of PWM outputs and glitch-free logic outputs. Each PWM output has an individual 4-bit intensity control (Table 14). When all outputs are to be used with the same PWM setting, the outputs can be controlled together instead using the global intensity control (Table 13). Table 10 shows how to set up the MAX7315 to suit a particular application.

PWM Timing

The PWM control uses a 240-step PWM period, divided into 15 master intensity timeslots. Each master intensity timeslot is divided further into 16 PWM cycles (Figure 11).

The master intensity operates as a gate, allowing the individual output settings to be enabled from 1 to 15 timeslots per PWM period (Figures 12, 13, 14) (Table 13).

Each output's individual 4-bit intensity control only operates during the number of timeslots gated by the

master intensity. The individual controls provide 16 intensity settings from 1/16 through 16/16 (Table 14).

Figures 15, 16, and 17 show examples of individual intensity control settings. The highest value an individual or global setting can be set to is 16/16. This setting forces the output to ignore the master control, and follow the logic level set by the appropriate blink phase register bit. The output becomes a glitch-free static output with no PWM.

Using PWM Intensity Controls with Blink Disabled

When blink is disabled (Table 7), the blink phase 0 register specifies each output's logic level during the PWM on-time (Table 8). The effect of setting an output's blink phase 0 register bit to 0 or 1 is shown in Table 11. With its output bit set to zero, an LED can be controlled with 16 intensity settings from 1/16th duty through fully on, but cannot be turned fully off using the PWM intensity control. With its output bit set to 1, an LED can be controlled with 16 intensity settings from fully off through 15/16th duty.

Table 7. Blink Controls

| BLINK ENABLE FLAG E | BLINK FLIP FLAG B | BLINK FUNCTION | OUTPUT REGISTERS USED |
|---------------------|-------------------|----------------|------------------------|
| 0 | X | Disabled | Blink phase 0 register |
| 1 | 0 | Enabled | Blink phase 0 register |
| | 1 | | Blink phase 1 register |

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Using PWM Intensity Controls with Blink Enabled

When blink is enabled (Table 7), the blink phase 0 register and blink phase 1 register specify each output's logic level during the PWM on-time during the respective blink phases (Tables 8 and 9). The effect of setting an output's blink phase X register bit to 0 or 1 is shown in Table 12. LEDs can be flipped between either directly on and off, or between a variety of high/low PWM intensities.

Global/O8 Intensity Control

The 4 bits used for output O8's PWM individual intensity setting also double as the global intensity control (Table 13). Global intensity simplifies the PWM settings when the application requires them all to be the same, such as for backlight applications, by replacing the 9 individual settings with 1 setting. Global intensity is enabled with the global intensity flag G in the configuration register (Table 4). When global PWM control is used, the 4 bits of master intensity and 4 bits of O8 intensity effectively combine to provide an 8 bit, 240-step intensity control applying to all outputs.

It is not possible to apply global PWM control to a subset of the ports, and use the others as logic outputs. To mix static logic outputs and PWM outputs, individual PWM control must be selected (Table 10).

Applications Information

Output Level Translation

The open-drain output architecture allows the ports to level translate the outputs to higher or lower voltages than the MAX7315 supply. An external pullup resistor can be used on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to

5.5V. For interfacing CMOS inputs, a pullup resistor value of 220k Ω is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Compatibility with PCA9534 and PCA9554(A)

The MAX7315 is pin compatible and software compatible with PCA9534, and its variants PCA9554 and PCA9554A. However, some PCA9534 and PCA9554(A) functions are not implemented in the MAX7315, and the MAX7315's PWM and blink functionality is not supported in the PCA9534 and PCA9554(A). Software compatibility is clearly not 100%, but the MAX7315 was designed so the subset (omitted) features default to the same power-up behavior as the PCA9534 and PCA9554(A), and the superset features do not use existing registers in a different way. In practice, many applications can use the MAX7315 as a drop-in replacement for the PCA9534 or PCA9554(A) with no software change.

Driving LED Loads

When driving LEDs, a resistor in series with the LED must be used to limit the LED current to no more than 50mA. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).

V_{SUPPLY} is the supply voltage used to drive the LED (V).

V_{LED} is the forward voltage of the LED (V).

Table 8. Blink Phase 0 Register

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|---------------------------|-----|--------------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write outputs phase 0 | 0 | 0x01 | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| Read-back outputs phase 0 | 1 | | | | | | | | | |

Table 9. Blink Phase 1 Register

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|---------------------------|-----|--------------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write outputs phase 1 | 0 | 0x09 | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| Read-back outputs phase 1 | 1 | | | | | | | | | |

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Table 10. PWM Application Scenarios

| APPLICATION | RECOMMENDED CONFIGURATION |
|--|--|
| All outputs static without PWM | Set the master, O8 intensity register 0x0E to any value from 0x00 to 0x0F. The global intensity G bit in the configuration register is don't care. The output intensity registers 0x10 through 0x13 are don't care. |
| A mix of static and PWM outputs, with PWM outputs using different PWM settings | Set the master, O8 intensity register 0x0E to any value from 0x10 to 0xFF. Clear global intensity G bit to 0 in the configuration register to disable global intensity control. For the static outputs, set the output intensity value to 0xF. For the PWM outputs, set the output intensity value in the range 0x0 to 0xE. |
| A mix of static and PWM outputs, with PWM outputs all using the same PWM setting | As above. Global intensity control cannot be used with a mix of static and PWM outputs, so write the individual intensity registers with the same PWM value. |
| All outputs PWM using the same PWM setting | Set the master, O8 intensity register 0x0E to any value from 0x10 to 0xFF. Set global intensity G bit to 1 in the configuration register to enable global intensity control. The master, O8 intensity register 0x0E is the only intensity register used. The output intensity registers 0x10 through 0x13 are don't care. |

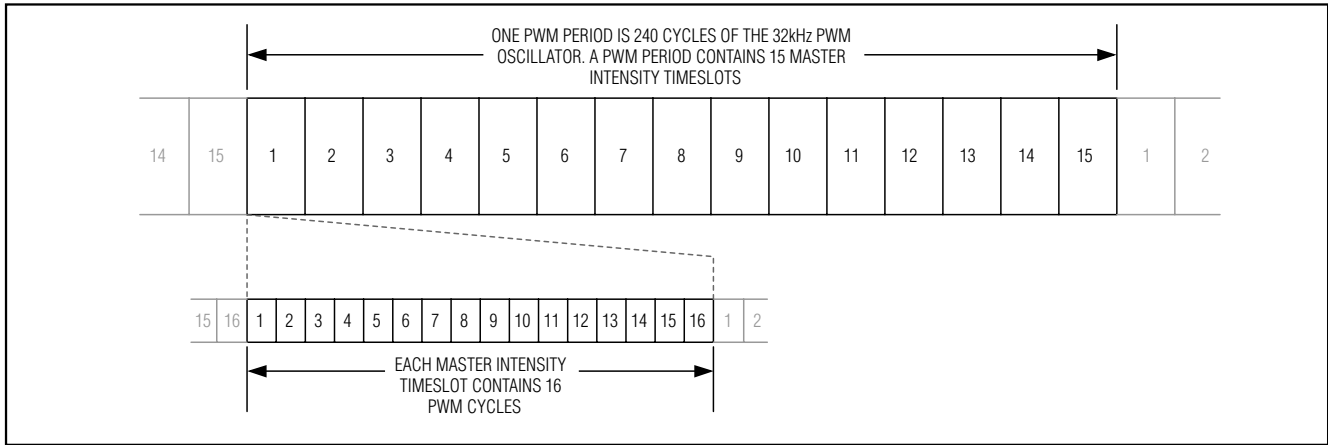


Figure 11. PWM Timing

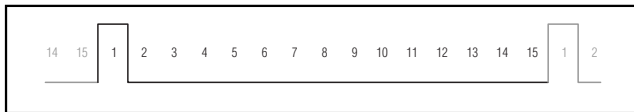


Figure 12. Master Set to 1/15

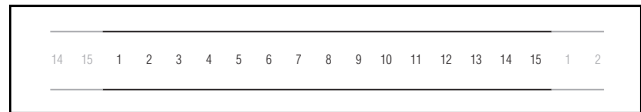


Figure 14. Master Set to 15/15

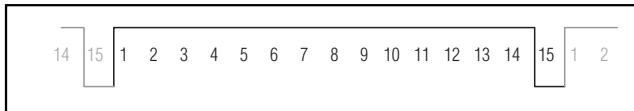


Figure 13. Master Set to 14/15

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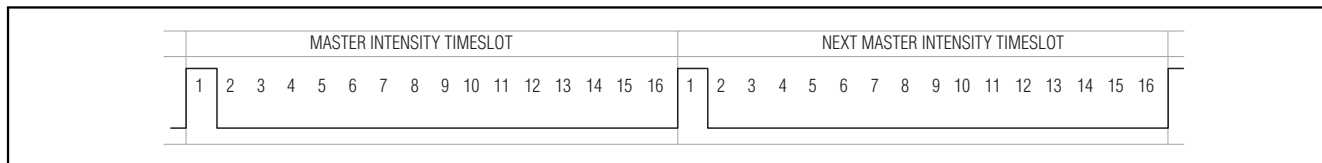


Figure 15. Individual (or Global) Set to 1/16

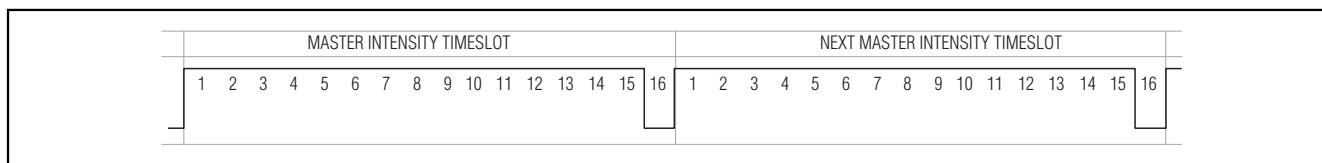


Figure 16. Individual (or Global) Set to 15/16

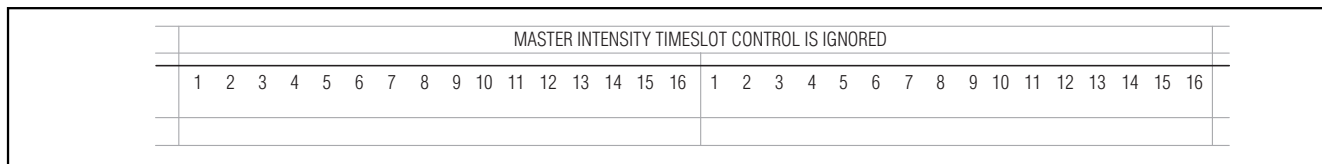


Figure 17. Individual (or Global) Set to 16/16

Table 11. PWM Intensity Settings (Blink Disabled)

| OUTPUT (OR GLOBAL) INTENSITY SETTING | PWM DUTY CYCLE OUTPUT BLINK PHASE 0 REGISTER BIT = 0 | | LED BEHAVIOR WHEN OUTPUT BLINK PHASE 0 REGISTER BIT = 0 (LED IS ON WHEN OUTPUT IS LOW) | PWM DUTY CYCLE OUTPUT BLINK PHASE 0 REGISTER BIT = 1 | | LED BEHAVIOR WHEN OUTPUT BLINK PHASE 0 REGISTER BIT = 1 (LED IS ON WHEN OUTPUT IS LOW) |
|--|--|------------|--|--|-----------------------|--|
| | LOW TIME | HIGH TIME | | LOW TIME | HIGH TIME | |
| 0x0 | 1/16 | 15/16 | ← Increasing PWM intensity | 15/16 | 1/16 | Increasing PWM intensity → |
| 0x1 | 2/16 | 14/16 | | 14/16 | 2/16 | |
| 0x2 | 3/16 | 13/16 | | 13/16 | 3/16 | |
| 0x3 | 4/16 | 12/16 | | 12/16 | 4/16 | |
| 0x4 | 5/16 | 11/16 | | 11/16 | 5/16 | |
| 0x5 | 6/16 | 10/16 | | 10/16 | 6/16 | |
| 0x6 | 7/16 | 9/16 | | 9/16 | 7/16 | |
| 0x7 | 8/16 | 8/16 | | 8/16 | 8/16 | |
| 0x8 | 9/16 | 7/16 | | 7/16 | 9/16 | |
| 0x9 | 10/16 | 6/16 | | 6/16 | 10/16 | |
| 0xA | 11/16 | 5/16 | | 5/16 | 11/16 | |
| 0xB | 12/16 | 4/16 | | 4/16 | 12/16 | |
| 0xC | 13/16 | 3/16 | | 3/16 | 13/16 | |
| 0xD | 14/16 | 2/16 | | 2/16 | 14/16 | |
| 0xE | 15/16 | 1/16 | Highest PWM intensity | 1/16 | 15/16 | Lowest PWM intensity |
| 0xF | Static low | Static low | Full intensity, no PWM (LED on continuously) | Static high impedance | Static high impedance | LED off continuously |

8-Port I/O Expander with LED Intensity Control and Interrupt

V_{OL} is the output low voltage of the MAX7313 when sinking I_{LED} (V).

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 14mA from a 5V supply, $R_{LED} = (5 - 2.2 - 0.25) / 0.014 = 182\Omega$.

Driving Load Currents Higher than 50mA

The MAX7315 can be used to drive loads drawing more than 50mA, like relays and high-current white LEDs, by paralleling outputs. Use at least one output per 50mA of load current; for example, a 5V 330mW relay draws 66mA and needs two paralleled outputs to drive it. Ensure that the paralleled outputs chosen are controlled by the same blink phase register, i.e., select outputs from the P0 through P7 range. This way, the paralleled outputs are turned on and off together. Do not use output O8 as part of a load-sharing design. O8 cannot be switched at the same time as any of the other outputs because it is controlled by a different register.

The MAX7315 must be protected from the negative voltage transient generated when switching off induc-

tive loads, such as relays, by connecting a reverse-biased diode across the inductive load (Figure 18). The peak current through the diode is the inductive load's operating current.

Power-Supply Considerations

The MAX7315 operates with a power-supply voltage of 2V to 3.6V. Bypass the power supply to GND with at least 0.047 μ F as close to the device as possible.

Chip Information

TRANSISTOR COUNT: 17,611

PROCESS: BiCMOS

Table 12. PWM Intensity Settings (Blink Enabled)

| OUTPUT (OR GLOBAL) INTENSITY SETTING | PWM DUTY CYCLE OUTPUT BLINK PHASE X REGISTER BIT = 0 | | PWM DUTY CYCLE OUTPUT BLINK PHASE X REGISTER BIT = 1 | | EXAMPLES OF LED BLINK BEHAVIOR (LED IS ON WHEN OUTPUT IS LOW) | |
|--|---|--------------|---|-----------------------|---|---|
| | LOW TIME | HIGH TIME | LOW TIME | HIGH TIME | BLINK PHASE 0 REGISTER BIT = 0 | BLINK PHASE 0 REGISTER BIT = 1 |
| | | | | | BLINK PHASE 1 REGISTER BIT = 1 | BLINK PHASE 1 REGISTER BIT = 0 |
| 0x0 | 1/16 | 15/16 | 15/16 | 1/16 | Phase 0: LED on at low intensity Phase 1: LED on at high intensity | Phase 0: LED on at high intensity Phase 1: LED on at low intensity |
| 0x1 | 2/16 | 14/16 | 14/16 | 2/16 | | |
| 0x2 | 3/16 | 13/16 | 13/16 | 3/16 | | |
| 0x3 | 4/16 | 12/16 | 12/16 | 4/16 | | |
| 0x4 | 5/16 | 11/16 | 11/16 | 5/16 | | |
| 0x5 | 6/16 | 10/16 | 10/16 | 6/16 | | |
| 0x6 | 7/16 | 9/16 | 9/16 | 7/16 | | |
| 0x7 | 8/16 | 8/16 | 8/16 | 8/16 | Output is half intensity during both blink phases | |
| 0x8 | 9/16 | 7/16 | 7/16 | 9/16 | Phase 0: LED on at high intensity Phase 1: LED on at low intensity | Phase 0: LED on at low intensity Phase 1: LED on at high intensity |
| 0x9 | 10/16 | 6/16 | 6/16 | 10/16 | | |
| 0xA | 11/16 | 5/16 | 5/16 | 11/16 | | |
| 0xB | 12/16 | 4/16 | 4/16 | 12/16 | | |
| 0xC | 13/16 | 3/16 | 3/16 | 13/16 | | |
| 0xD | 14/16 | 2/16 | 2/16 | 14/16 | | |
| 0xE | 15/16 | 1/16 | 1/16 | 15/16 | Phase 0: LED on continuously Phase 1: LED off continuously | Phase 0: LED off continuously Phase 1: LED on continuously |
| 0xF | Static low | Static low | Static high impedance | Static high impedance | | |

8-Port I/O Expander with LED Intensity Control and Interrupt

MAX7315

Table 13. Master, O8 Intensity Register

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|---|-----|--------------------|-------------------------|----|----|----|---------------------|----|----|----|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MASTER AND GLOBAL INTENSITY | | | MSB MASTER INTENSITY | | | | LSB O8 INTENSITY | | | |
| Write master and global intensity | 0 | 0X0E | M3 | M2 | M1 | M0 | G3 | G2 | G1 | G0 |
| Read back master and global intensity | 1 | | 0 | 0 | 0 | 0 | — | — | — | — |
| Master intensity duty cycle is 0/15 (off); internal oscillator is disabled; all outputs will be static with no PWM | — | | 0 | 0 | 0 | 1 | — | — | — | — |
| Master intensity duty cycle is 1/15 | — | | 0 | 0 | 1 | 0 | — | — | — | — |
| Master intensity duty cycle is 2/15 | — | | 0 | 0 | 1 | 1 | — | — | — | — |
| Master intensity duty cycle is 3/15 | — | | — | — | — | — | — | — | — | — |
| — | — | | 1 | 1 | 0 | 1 | — | — | — | — |
| Master intensity duty cycle is 13/15 | — | | 1 | 1 | 1 | 0 | — | — | — | — |
| Master intensity duty cycle is 14/15 | — | | 1 | 1 | 1 | 1 | — | — | — | — |
| Master intensity duty cycle is 15/15 (full) | — | | — | — | — | — | 0 | 0 | 0 | 0 |
| — | — | | — | — | — | — | 0 | 0 | 0 | 1 |
| O8 intensity duty cycle is 1/16 | — | | — | — | — | — | 0 | 0 | 1 | 0 |
| O8 intensity duty cycle is 2/16 | — | | — | — | — | — | — | — | — | — |
| O8 intensity duty cycle is 3/16 | — | | — | — | — | — | 1 | 1 | 0 | 1 |
| — | — | | — | — | — | — | 1 | 1 | 1 | 0 |
| O8 intensity duty cycle is 14/16 | — | | — | — | — | — | 1 | 1 | 1 | 1 |
| O8 intensity duty cycle is 15/16 | — | | — | — | — | — | — | — | — | — |
| O8 intensity duty cycle is 16/16 (static output, no PWM) | — | — | — | — | — | 1 | 1 | 1 | 1 | |

8-Port I/O Expander with LED Intensity Control and Interrupt

Table 14. Output Intensity Registers

| REGISTER | R/W | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | |
|--|-----|--------------------|---|------|------|------|----------------------------|------|------|------|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OUTPUTS P1, P0 INTENSITY | | 0x10 | MSB | | | | LSB | | | |
| | | | OUTPUT P1 INTENSITY | | | | OUTPUT P0 INTENSITY | | | |
| Write output P1, P0 intensity | 0 | | P1I3 | P1I2 | P1I1 | P1I0 | P0I3 | P0I2 | P0I1 | P0I0 |
| Read back output P1, P0 intensity | 1 | | 0 | 0 | 0 | 0 | — | — | — | — |
| Output P1 intensity duty cycle is 1/16 | — | | 0 | 0 | 0 | 1 | — | — | — | — |
| Output P1 intensity duty cycle is 2/16 | — | | 0 | 0 | 1 | 0 | — | — | — | — |
| Output P1 intensity duty cycle is 3/16 | — | | — | — | — | — | — | — | — | — |
| — | — | | — | — | — | — | — | — | — | — |
| Output P1 intensity duty cycle is 14/16 | — | | 1 | 1 | 0 | 1 | — | — | — | — |
| Output P1 intensity duty cycle is 15/16 | — | | 1 | 1 | 1 | 0 | — | — | — | — |
| Output P1 intensity duty cycle is 16/16 (static logic level, no PWM) | — | | 1 | 1 | 1 | 1 | — | — | — | — |
| — | — | | — | — | — | — | — | — | — | — |
| Output P0 intensity duty cycle is 1/16 | — | | — | — | — | — | 0 | 0 | 0 | 0 |
| Output P0 intensity duty cycle is 2/16 | — | | — | — | — | — | 0 | 0 | 0 | 1 |
| Output P0 intensity duty cycle is 3/16 | — | | — | — | — | — | 0 | 0 | 1 | 0 |
| — | — | | — | — | — | — | — | — | — | — |
| Output P0 intensity duty cycle is 14/16 | — | — | — | — | — | 1 | 1 | 0 | 1 | |
| Output P0 intensity duty cycle is 15/16 | — | — | — | — | — | 1 | 1 | 1 | 0 | |
| Output P0 intensity duty cycle is 16/16 (static logic level, no PWM) | — | — | — | — | — | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | |
| OUTPUTS P3, P2 INTENSITY | | 0x11 | MSB | | | | LSB | | | |
| | | | OUTPUT P3 INTENSITY | | | | OUTPUT P2 INTENSITY | | | |
| Write output P3, P2 intensity | 0 | P3I3 | P3I2 | P3I1 | P3I0 | P2I3 | P2I2 | P2I1 | P2I0 | |
| Read back output P3, P2 intensity | 1 | | | | | | | | | |
| | | | | | | | | | | |
| OUTPUTS P5, P4 INTENSITY | | 0x12 | MSB | | | | LSB | | | |
| | | | OUTPUT P5 INTENSITY | | | | OUTPUT P4 INTENSITY | | | |
| Write output P5, P4 intensity | 0 | P5I3 | P5I2 | P5I1 | P5I0 | P4I3 | P4I2 | P4I1 | P4I0 | |
| Read back output P5, P4 intensity | 1 | | | | | | | | | |
| | | | | | | | | | | |
| OUTPUTS P7, P6 INTENSITY | | 0x13 | MSB | | | | LSB | | | |
| | | | OUTPUT P7 INTENSITY | | | | OUTPUT P6 INTENSITY | | | |
| Write output P7, P6 intensity | 0 | P7I3 | P7I2 | P7I1 | P7I0 | P6I3 | P6I2 | P6I1 | P6I0 | |
| Read back output P7, P6 intensity | 1 | | | | | | | | | |
| | | | | | | | | | | |
| OUTPUT O8 INTENSITY | | | See the master, O8 intensity register (Table 13). | | | | | | | |

8-Port I/O Expander with LED Intensity Control and Interrupt

Table 15. MAX7311, PCA9535, and PCA9555 Register Compatibility

| PCA9534, PCA9554(A) REGISTER | ADDRESS | MAX7313 IMPLEMENTATION | MAX7311, PCA9535, PCA9555 IMPLEMENTATION | COMMENTS |
|------------------------------|-----------|--|--|--|
| Inputs | 0x00 | Inputs registers | Implemented | Same functionality |
| Outputs | 0x01 | Blink phase 0 registers | Implemented | Same functionality |
| Polarity inversion | 0x02 | Not implemented; register writes are ignored; register reads return 0x00 | Implemented; power-up default is 0x00 | If polarity inversion feature is unused, MAX7313 defaults to correct state |
| Configuration | 0x03 | Ports configuration registers | Not implemented | Same functionality |
| No registers | 0x0B | Blink phase 1 registers | Not implemented | Power-up default disables the blink and intensity (PWM) features |
| No register | 0x0E | Master and global/O8 intensity register | Not implemented | |
| No register | 0x0F | Configuration register | Not implemented | |
| No registers | 0x10–0x13 | Outputs intensity registers | Not implemented | |

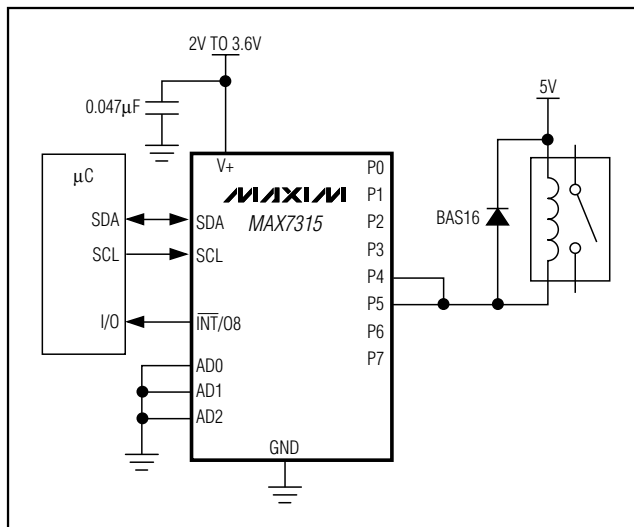
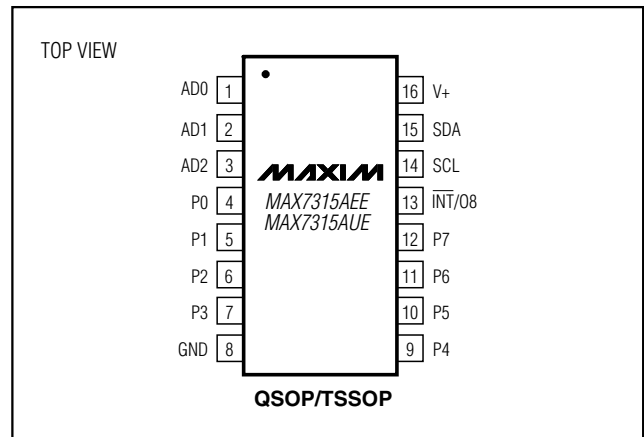


Figure 18. Diode-Protected Switching Inductive Load

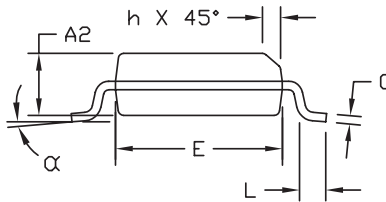
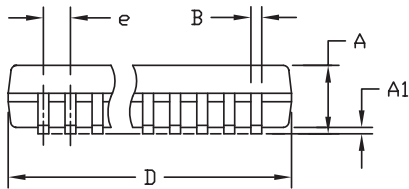
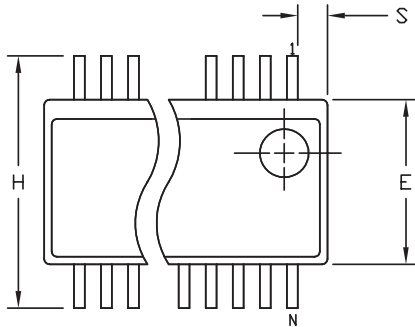
Pin Configurations (continued)



8-Port I/O Expander with LED Intensity Control and Interrupt

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



| DIM | INCHES | | MILLIMETERS | |
|-----|----------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .061 | .068 | 1.55 | 1.73 |
| A1 | .004 | .0098 | 0.102 | 0.249 |
| A2 | .055 | .061 | 1.40 | 1.55 |
| B | .008 | .012 | 0.20 | 0.30 |
| C | .0075 | .0098 | 0.191 | 0.249 |
| D | SEE VARIATIONS | | | |
| E | .150 | .157 | 3.81 | 3.99 |
| e | .025 BSC | | 0.635 BSC | |
| H | .230 | .244 | 5.84 | 6.20 |
| h | .010 | .016 | 0.25 | 0.41 |
| L | .016 | .035 | 0.41 | 0.89 |
| N | SEE VARIATIONS | | | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS:

| DIM | INCHES | | MILLIMETERS | | N |
|-----|--------|-------|-------------|-------|-------|
| | MIN. | MAX. | MIN. | MAX. | |
| D | .189 | .196 | 4.80 | 4.98 | 16 AB |
| S | .0020 | .0070 | 0.05 | 0.18 | |
| D | .337 | .344 | 8.56 | 8.74 | 20 AD |
| S | .0500 | .0550 | 1.270 | 1.397 | |
| D | .337 | .344 | 8.56 | 8.74 | 24 AE |
| S | .0250 | .0300 | 0.635 | 0.762 | |
| D | .386 | .393 | 9.80 | 9.98 | 28 AF |
| S | .0250 | .0300 | 0.635 | 0.762 | |

NOTES:

- 1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
- 2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
- 3). CONTROLLING DIMENSIONS: INCHES.
- 4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR **MAXIM**
 PROPRIETARY INFORMATION
 TITLE:
 PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH
 APPROVAL: _____ DOCUMENT CONTROL NO. 21-0055 REV. E 1/1

QSOP, EPS

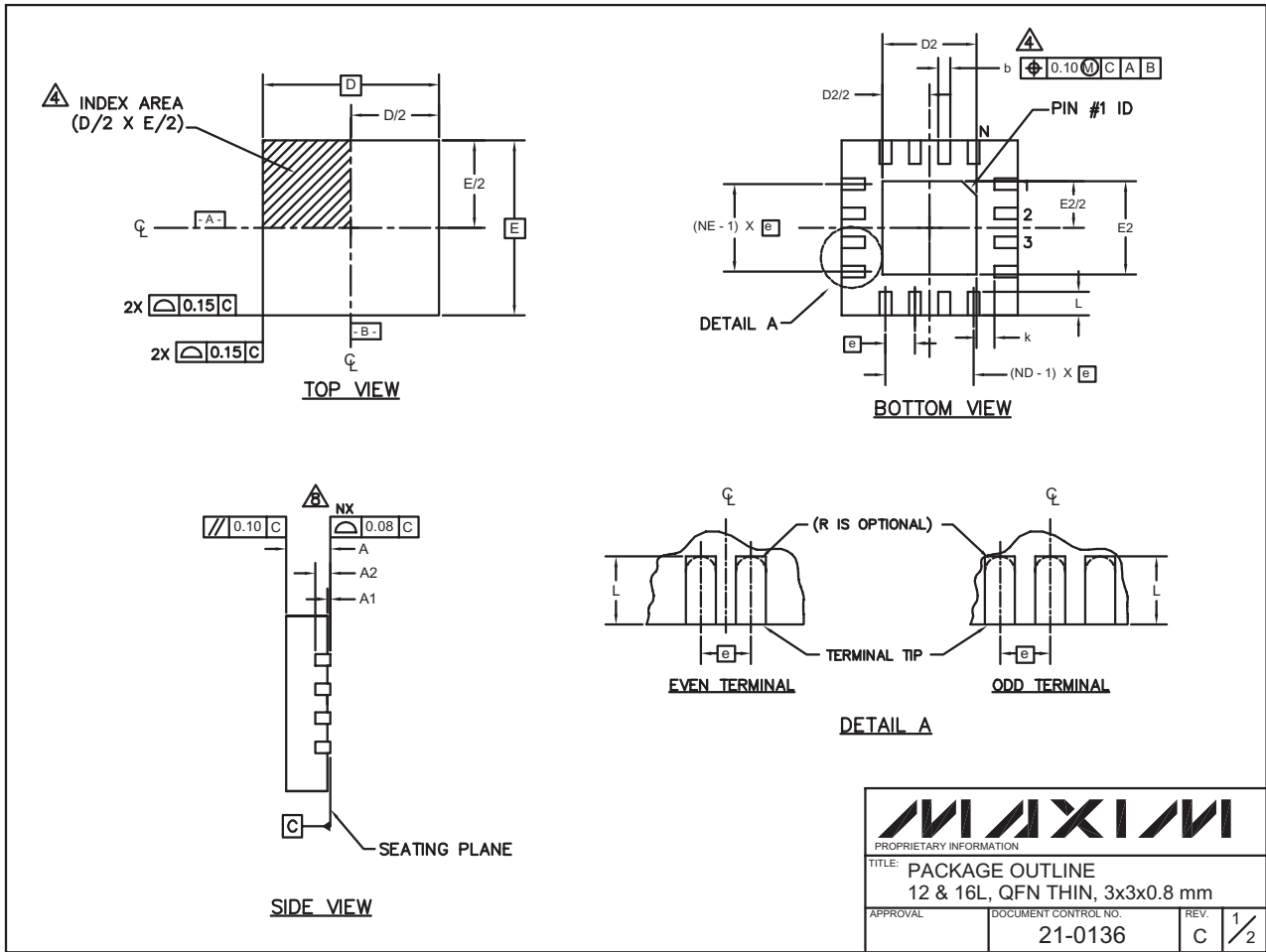
8-Port I/O Expander with LED Intensity Control and Interrupt

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX7315

12x16L QFN THIN.EPS



8-Port I/O Expander with LED Intensity Control and Interrupt

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

| PKG | 12L 3x3 | | | 16L 3x3 | | |
|------|-----------|------|------|-----------|------|------|
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| b | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC. | | | 0.50 BSC. | | |
| L | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | |
| ND | 3 | | | 4 | | |
| NE | 3 | | | 4 | | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | |
| k | 0.25 | - | - | 0.25 | - | - |

| EXPOSED PAD VARIATIONS | | | | | | | | |
|------------------------|------|------|------|------|------|------|-------------|--------|
| PKG. CODES | D2 | | | E2 | | | PIN ID | JEDEC |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | | |
| T1233-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-1 |
| T1633-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 |
| T1633F-3 | 0.65 | 0.80 | 0.95 | 0.65 | 0.80 | 0.95 | 0.225 x 45° | - |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.

| | | | |
|---|--|--------------------------|-------------------------------------|
|  | | | |
| <small>PROPRIETARY INFORMATION</small> | | | |
| TITLE: PACKAGE OUTLINE 12 & 16L, QFN THIN, 3x3x0.8 mm | | | |
| <small>APPROVAL</small> | <small>DOCUMENT CONTROL NO.</small> 21-0136 | <small>REV.</small> C | <small>2</small> / <small>2</small> |

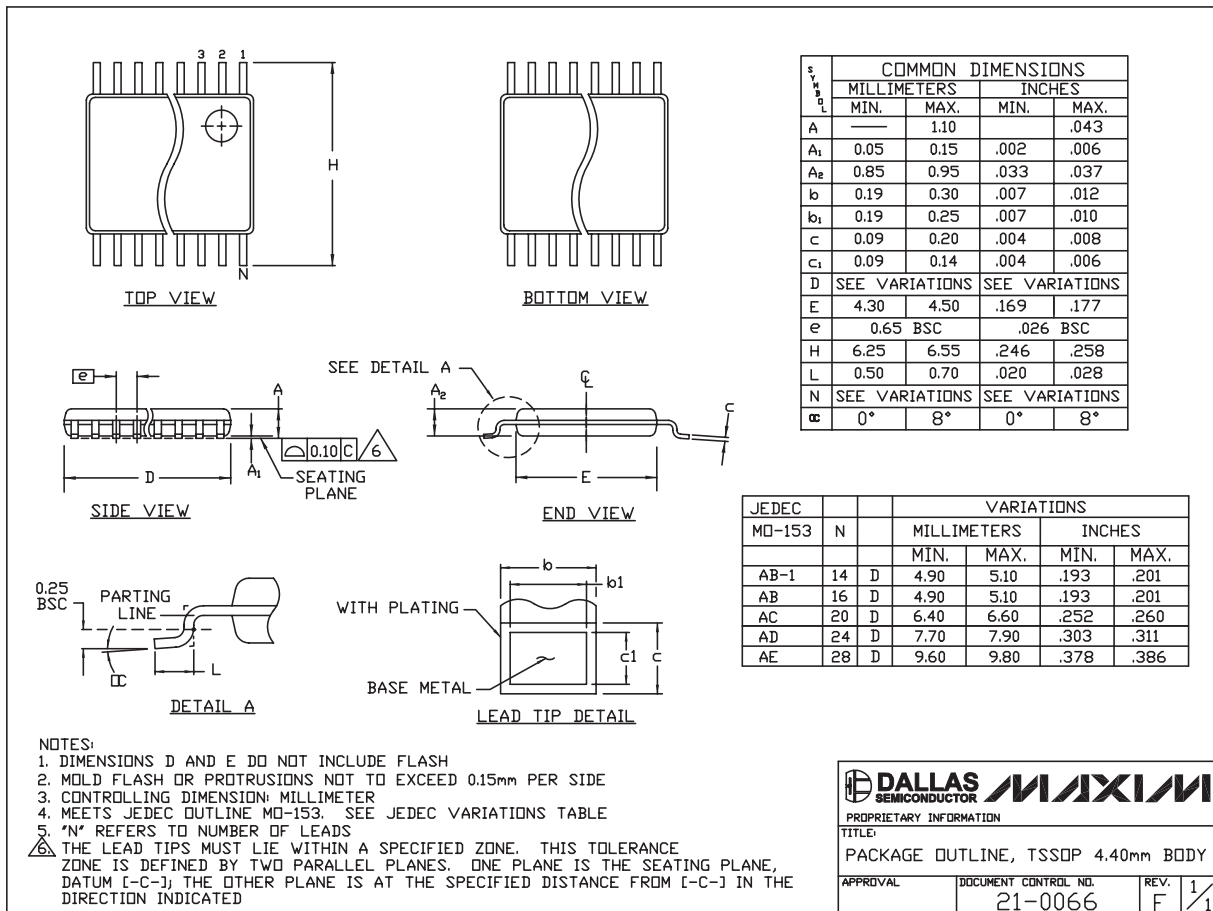
8-Port I/O Expander with LED Intensity Control and Interrupt

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX7315

TSSOP4_40mm.EPS



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